

MODEL NAME : VAW01
PROJECT CODE : ANRVAW0100
PCB NO : LA-9101P (Mars Pro)

DA60000UT00 LA-9101P M/B
DA40001FO00 LS-9101P POWER BUTTON/B
DA40001FP00 LS-9102P USB/B
DA40001FQ00 LS-9103P TP BUTTON/B



PCB VAW01 LA-9101P LS-9101P/9102P/9103P
DAZ0U500100



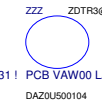
PCB VAW01 LA-9101P LS-9101P/9102P/9103P GOLD A31 !
DAZ0U500101



PCB VAW00 LA-9101P LS-9101P/9102P/9103P TRIPOD A31 !
DAZ0U500102



PCB VAW00 LA-9101P LS-9101P/9102P/9103P HANNSTARB A31 !
DAZ0U500103



PCB VAW00 LA-9101P LS-9101P/9102P/9103P ZDT A31 !
DAZ0U500104

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Schematic Document

Intel Chief River Ivy Bridge (BGA) + Panther Point OAK 15" UMA/DIS AMD Mars Pro

2012-08-22

Rev: 0.4

46@ : for 46 level

@ : Nopop Component

CONN@ : Connector Component

KB9012@ : ENE KB9012 Implemented

UMA@ : Only for UMA

EMC@ : EMI/ESD parts

GCLK@ : Green CLK implemented

GCLKUMA@ : Green CLK for UMA

GCLKDIS@ : Green CLK for DIS

XTAL@ : X'tal implemented

XTALDIS@ : X'tal with DIS implemented

R1@ : R1 P/N

R3@ : R3 P/N

i3R1@ : CPU i3-3217 1.8G

i3VOSR1@ : CPU i3-2365 1.4G

i5R1@ : CPU i5-3317 1.7G

i7R1@ : CPU i7-3517 1.9G

CEL1@ : CPU Celeron 887 1.5G

PENR1@ : CPU Pentium 997 1.6G

DIS@ : Only for Discrete

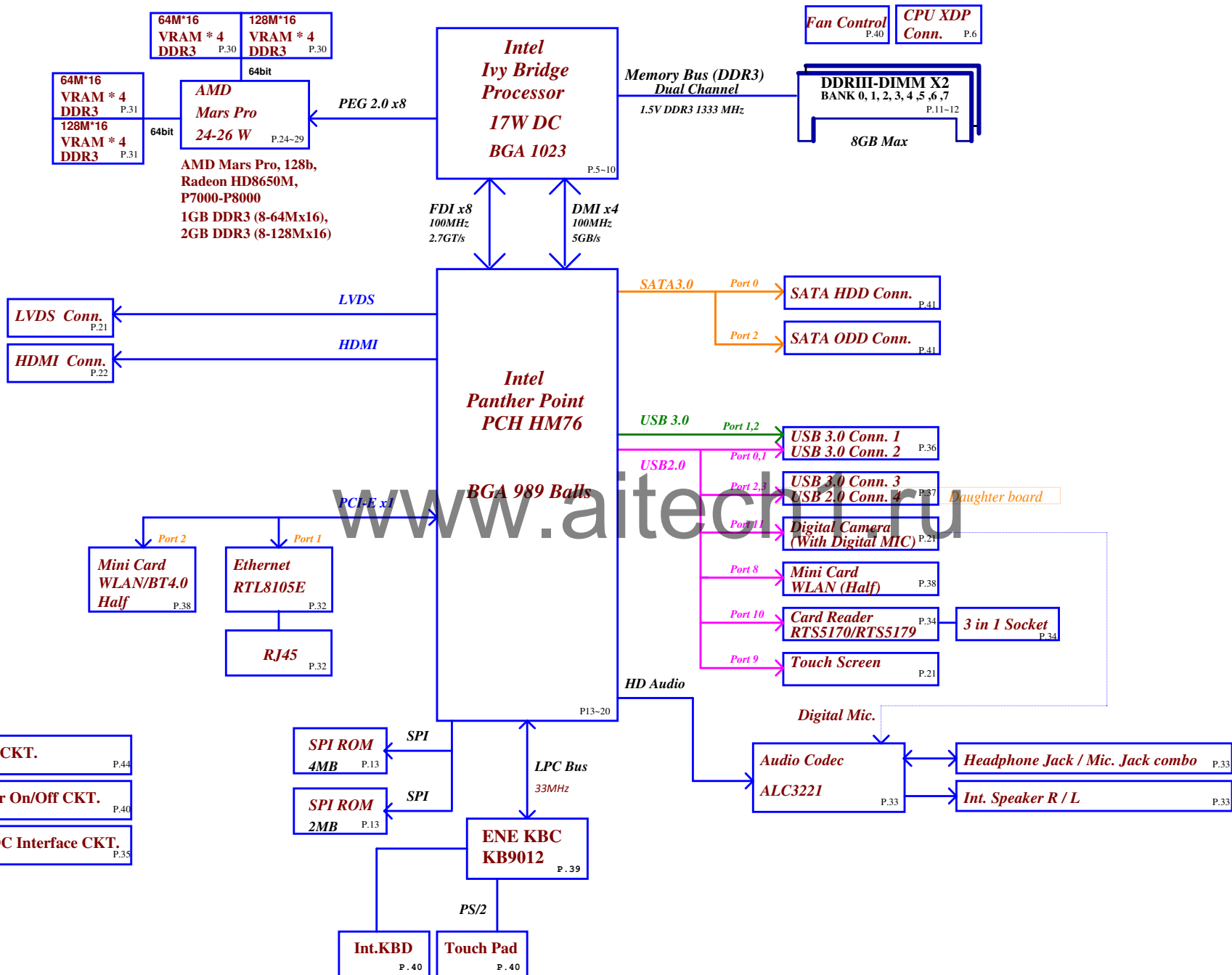
TH@/THR1@ : Thames-XT

MS@/MSR1@ : Mars Pro

X76@ :

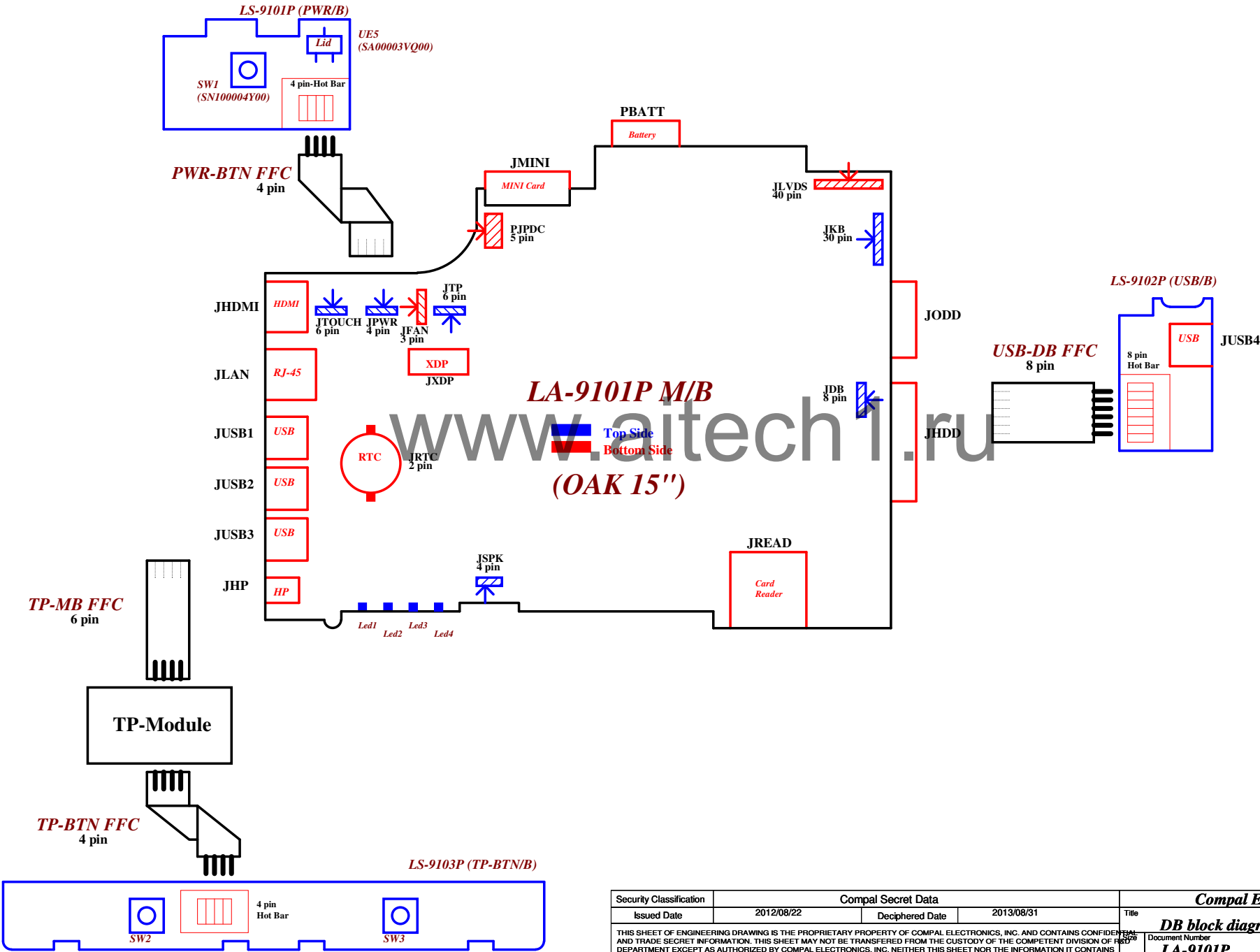
SPI-ROM & VRAM Group

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Issued Date	2012/08/22	Deciphered Date	2013/08/31	Title	Cover Page
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				Date	Wednesday, August 28, 2012
				Sheet	1 of 57
				Rev	0.4



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Project Code : VAW01
File Name : LA-9101P



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Issued Date	2012/08/22	Deciphered Date	2013/08/31	Title	DB block diagram
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				Date	Wednesday, August 29, 2012
				Sheet	3 of 57
				Rev	0.4

Board ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

ID	PCB Revision
0	0.1
1	0.1
2	0.2
3	0.2
4	0.3
5	0.4
6	1.0
7	1.0
UMA	THM
	MARS

Project ID Table

ID	Project Revision
0	
1	
2	
3	
4	
5	UMA
6	DIS THAMES
7	DIS MARS PRO

SMBUS Control Table

	SOURCE	MINI1	MINI2	BATT	SODIMM	Express Card	Thermal Sensor	FFS	VGA Thermal Sensor	VGA	XDP	Charger
EC_SMB_CK1 EC_SMB_DA1	KB9012			V								V
EC_SMB_CK2 EC_SMB_DA2	KB9012								V	V		
PCH_SML0CLK PCH_SML0DATA	PCH											
PCH_SML1CLK PCH_SML1DATA	PCH											
MEM_SMBCLK MEM_SMBDATA	PCH	V	V		V	V		V			V	

Link

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	10/100 LAN	CLKOUTFLEX0	None
	CLKOUT_PCIE1	MINI CARD WLAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	None	CLKOUTFLEX2	None
	CLKOUT_PCIE3	None	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC LPC
PCI2	None
PCI3	None
PCI4	None

SATA	DESTINATION
SATA0	HDD
SATA1	None
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

PCI EXPRESS	DESTINATION
Lane 1	10/100 LAN
Lane 2	MINI CARD (WLAN)
Lane 3	None
Lane 4	None
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

PCH

USB PORT#	DESTINATION
0	USB conn.2
1	USB conn.1
2	USB conn.3
3	USB conn.4 (DB)
4	NC
5	NC
6	NC
7	NC
8	MINI CARD (WLAN)
9	Touch Screen
10	Card Reader
11	Camera
12	NC
13	NC

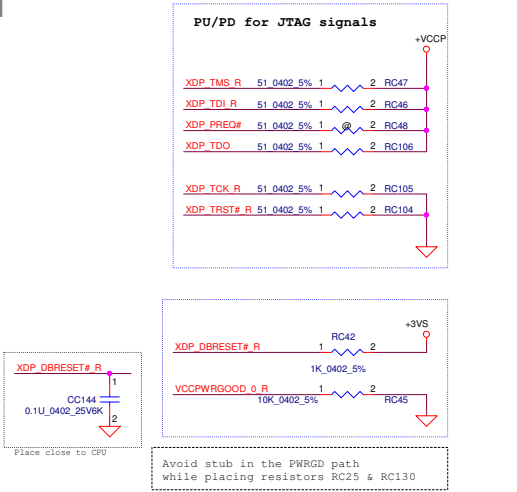
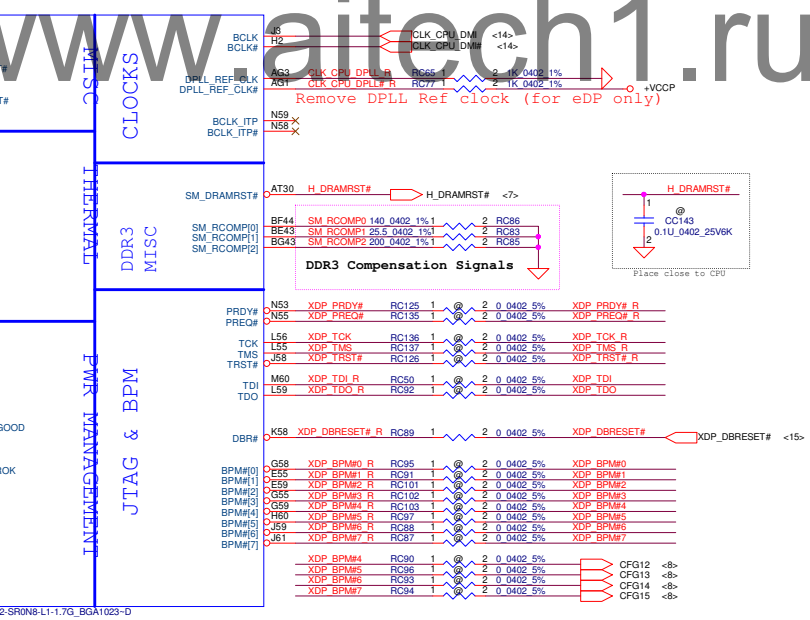
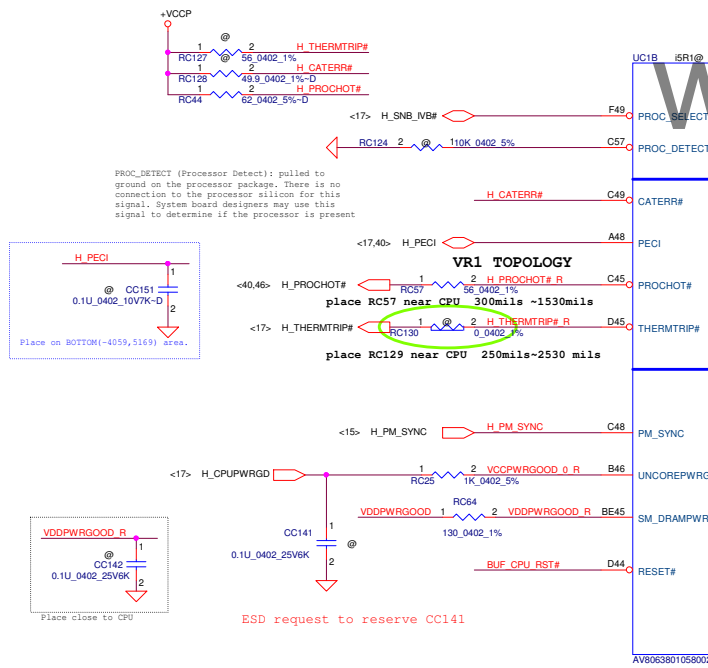
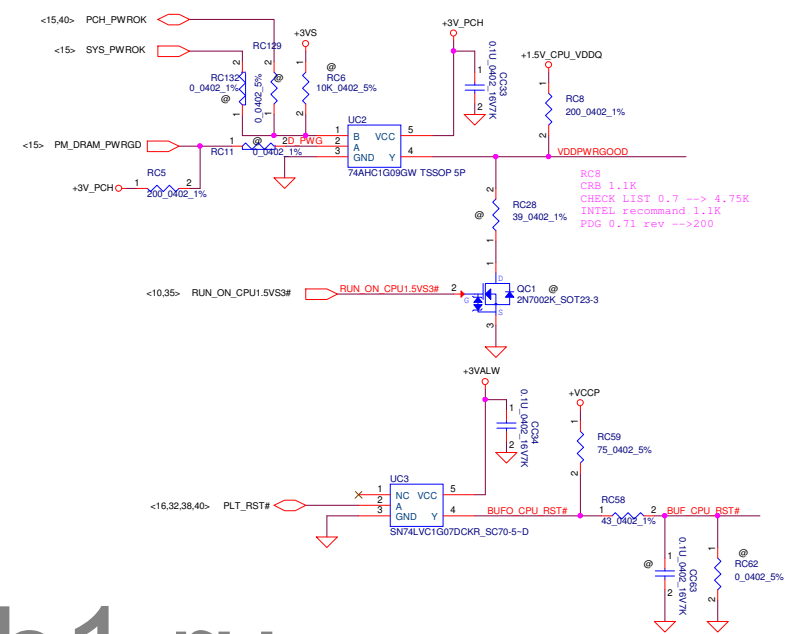
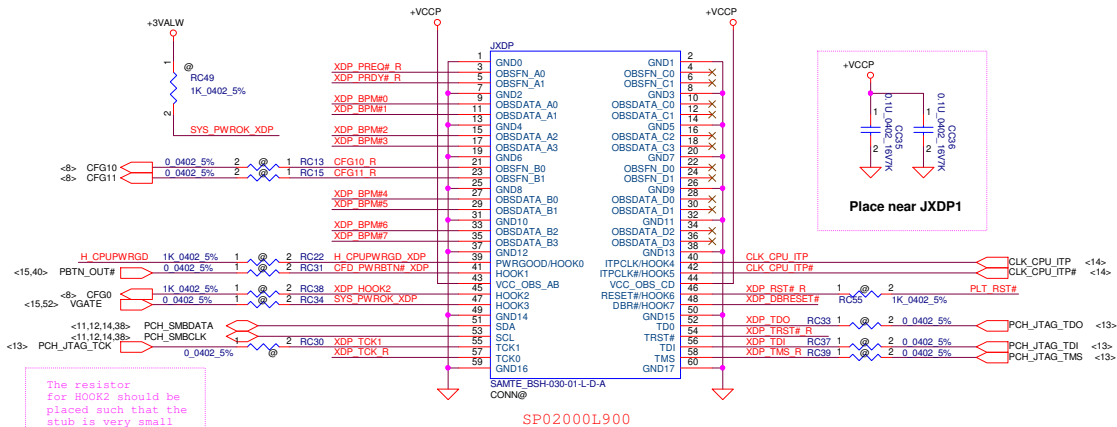
Symbol Note :

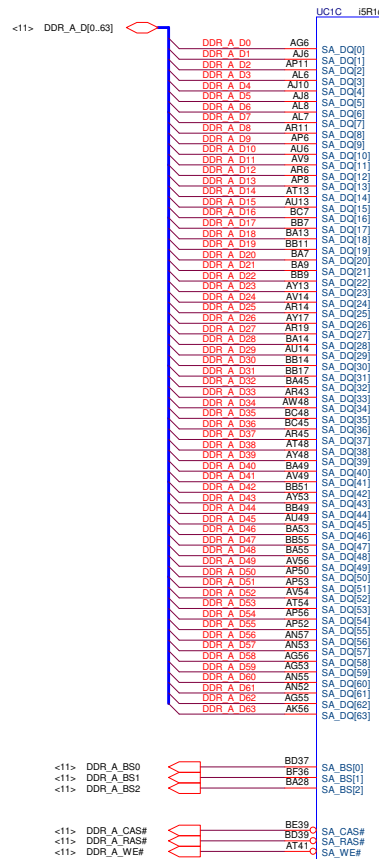


: means Digital Ground

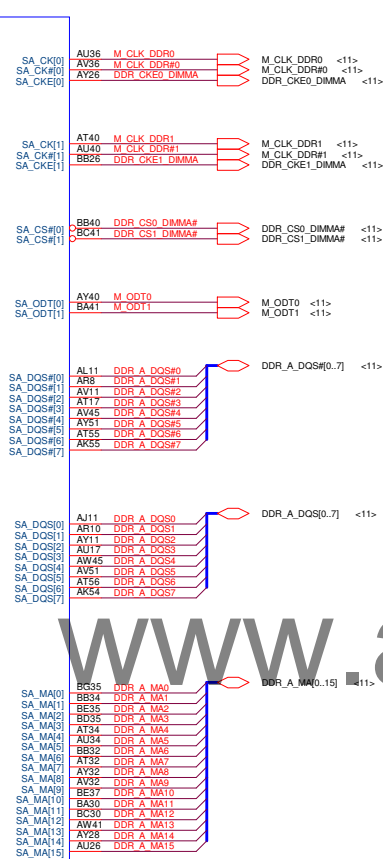


: means Analog Ground

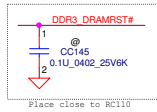
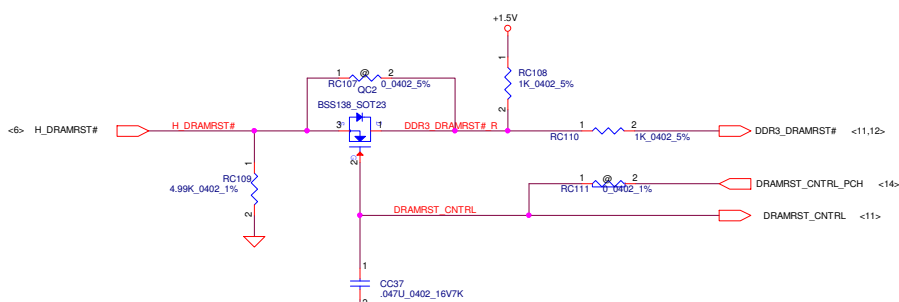
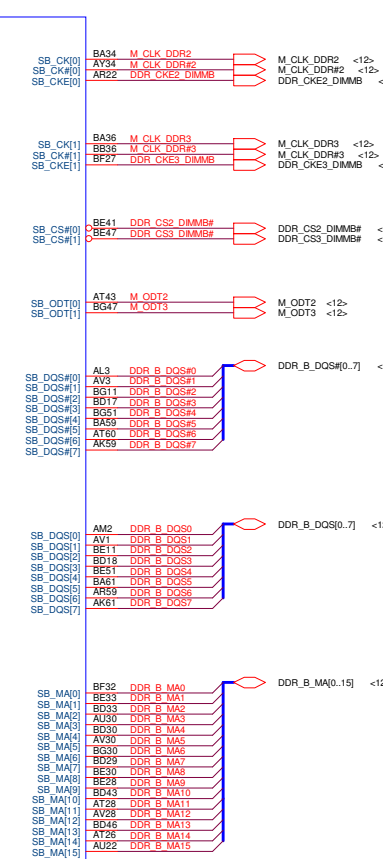


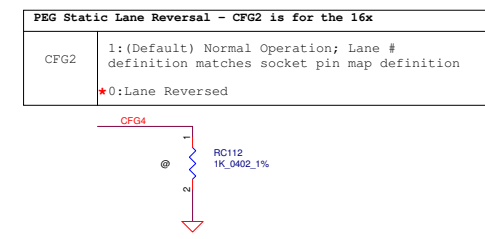


DDR SYSTEM MEMORY A

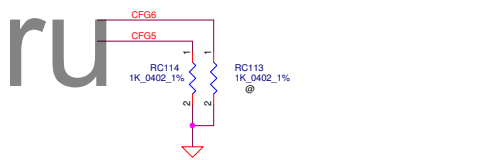


DDR SYSTEM MEMORY B

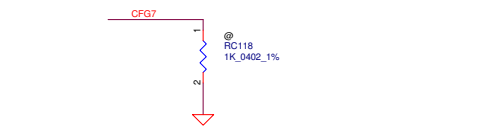




Display Port Presence Strap	
CFG4	<p>★ 1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>

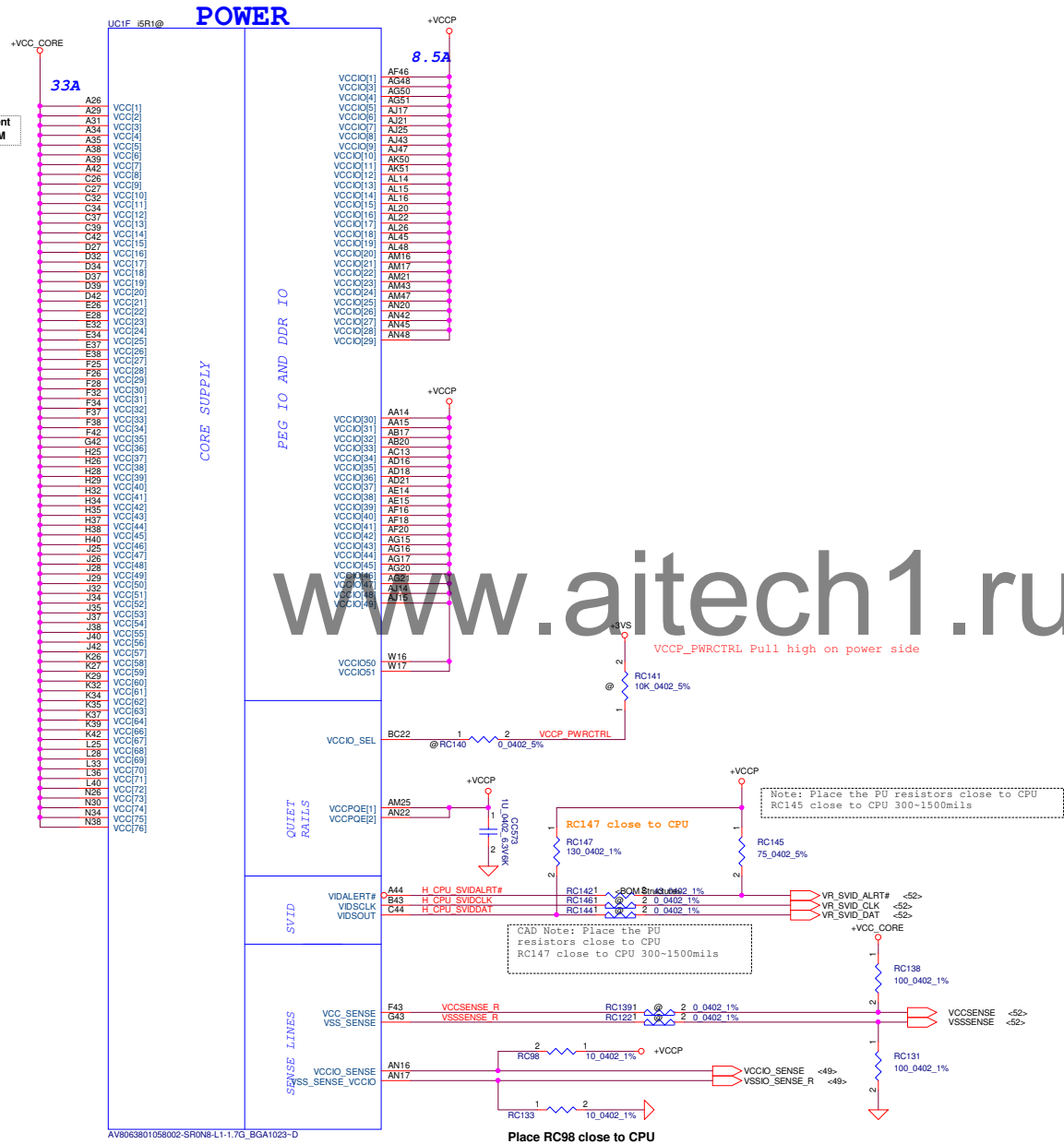


PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 *10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



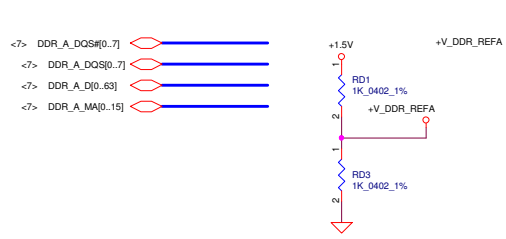
PEG DEFER TRAINING	
CFG7	<p>*1: (Default) PEG Train immediately following xxRESETB de assertion</p> <p>0: PEG Wait for BIOS for training</p>

ULV 17W , Max Current
in Turbo Mode or HFM



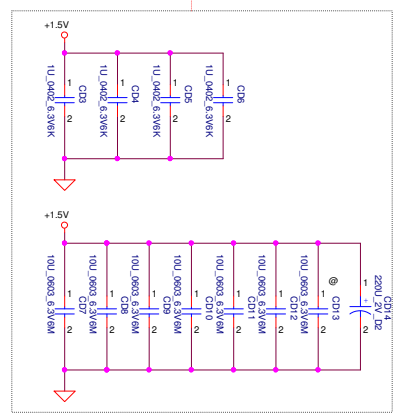
Iccmax current changed for PDDG Rev0.7

CPU Power Rail Table		
Voltage Rail	Voltage	50 Iccmax Current (A)
VCC	0.65-1.3	53
VCCIO	1.05/1	8.5
VAXG	0.0-1.1	33
VCCPLL	1.8	1.2
VDDQ	1.5	5
VCCSA	0.65-0.9	6
+1.5V_MEM	1.5	12-16 *
★ Description		
5A to Mem controller (+1.5V_CPU_VDDQ)		
5-6A to 2 DIMMs/channel		
2-5A to +1.5V_RUN & +0.75V_DDR_VTT		

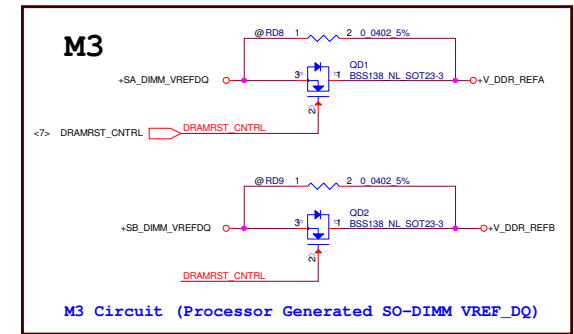
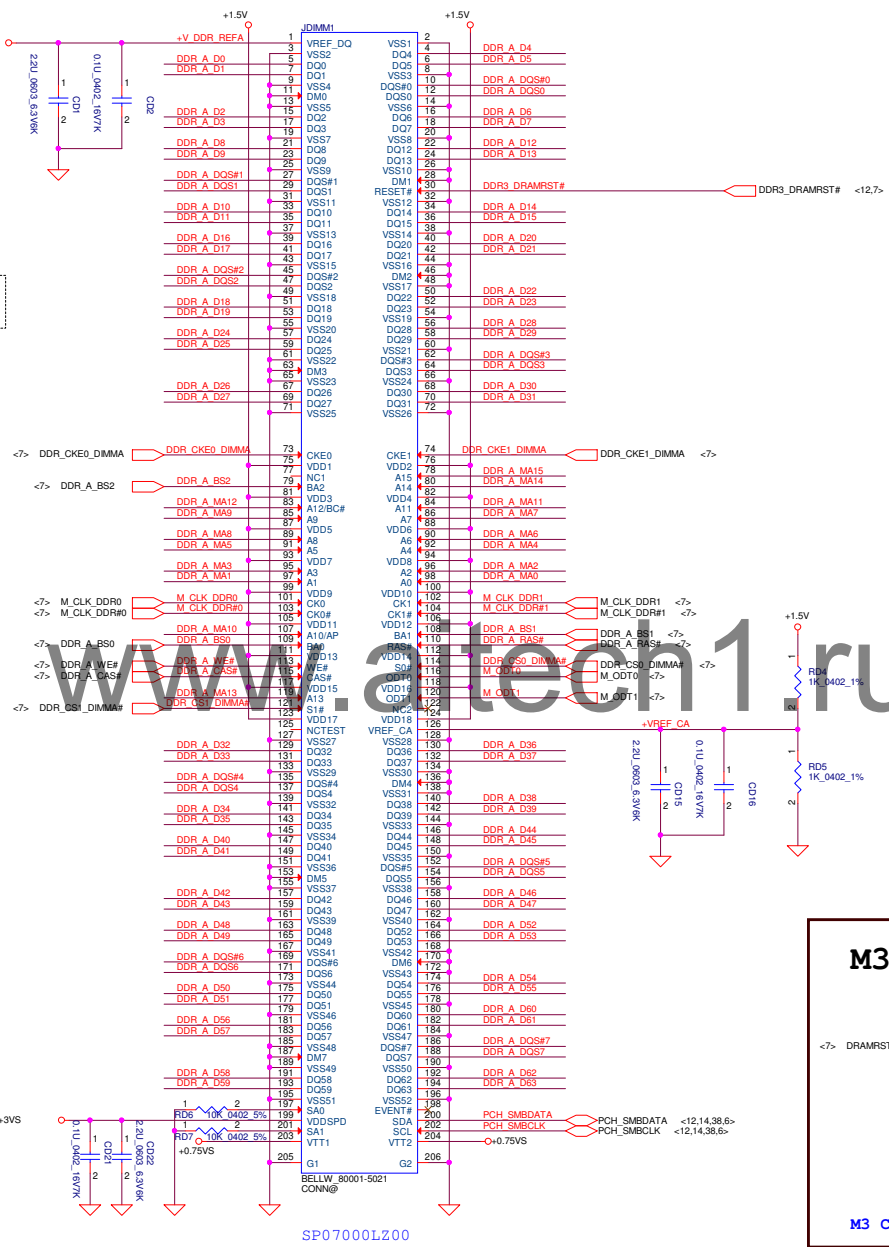
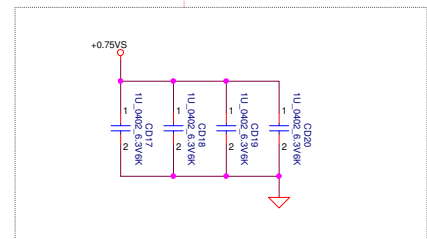


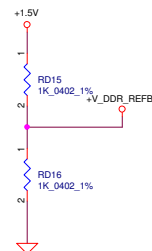
Layout Note:
Place near JDIMM1

All VREF traces should have 10 mil trace width

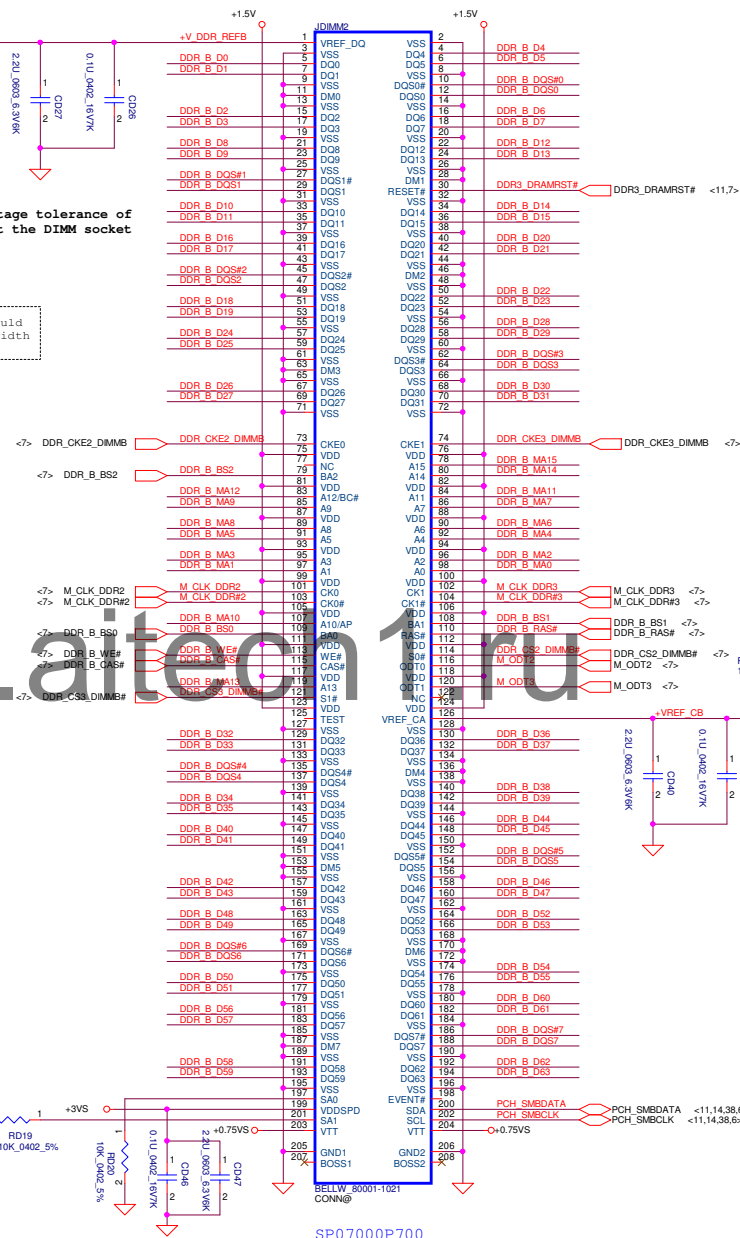


Layout Note:
Place near JDIMM1.203,204

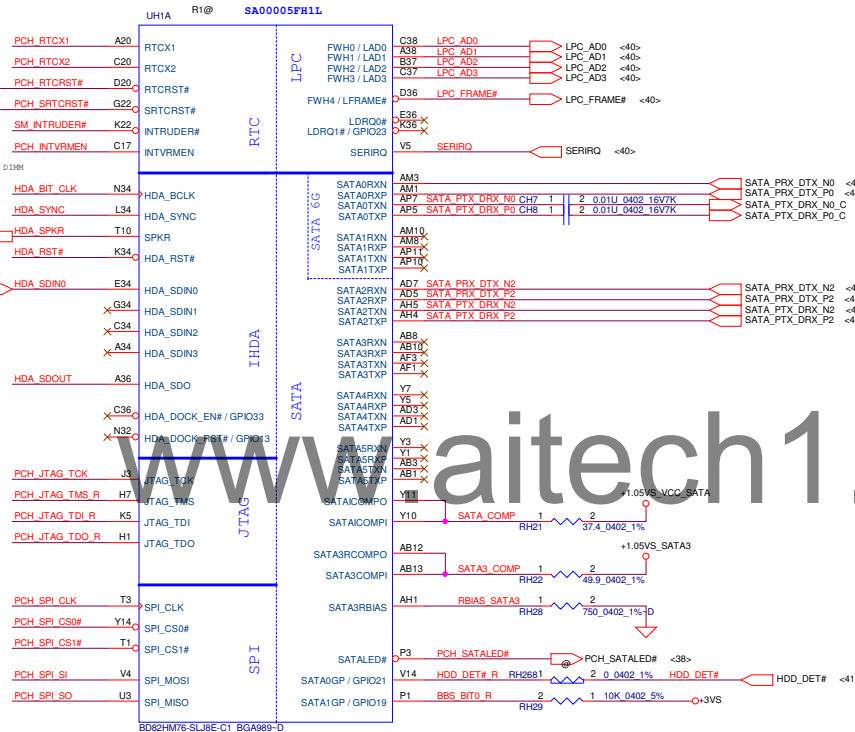
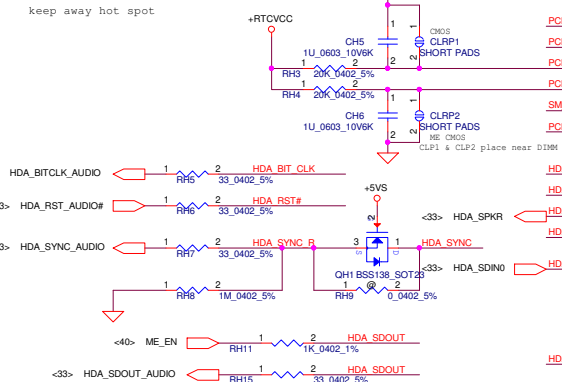
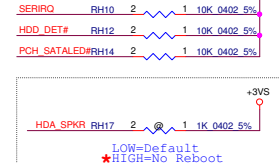
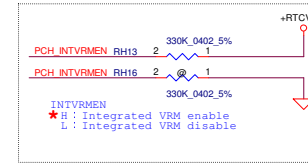
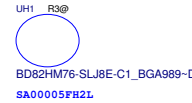
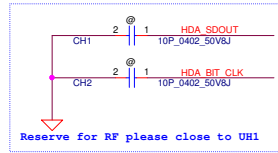
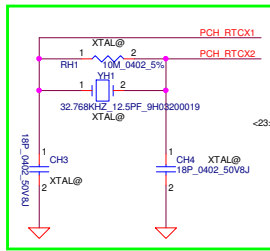




All VREF traces should have 10 mil trace width



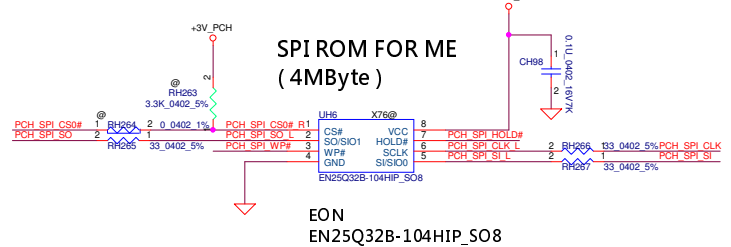
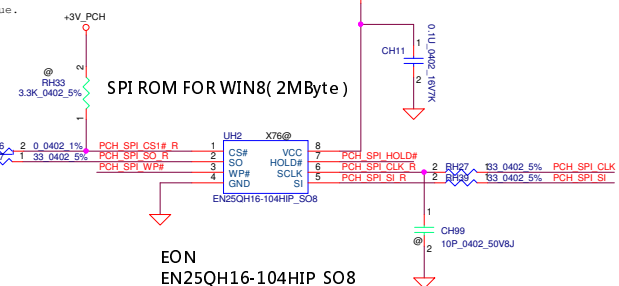
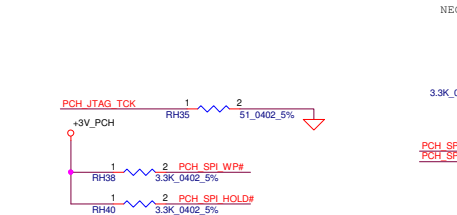
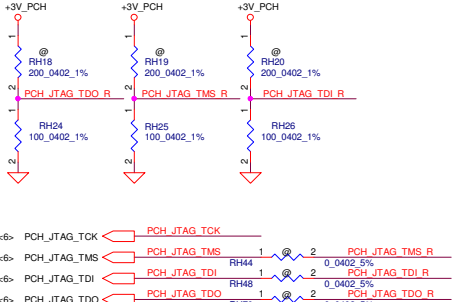
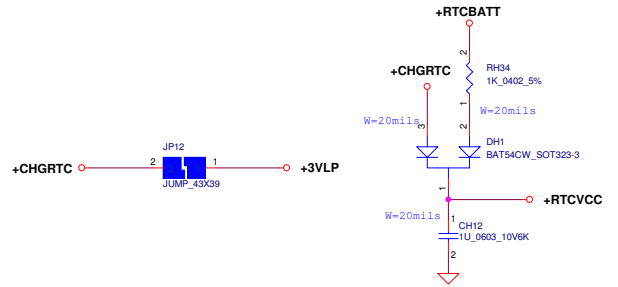
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Issued Date	2012/08/22	Deciphered Date	2013/08/31	Title	DDRIII DIMMB
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				LA-9101P	
				Date: Wednesday, August 29, 2012	Sheet 12 of 57



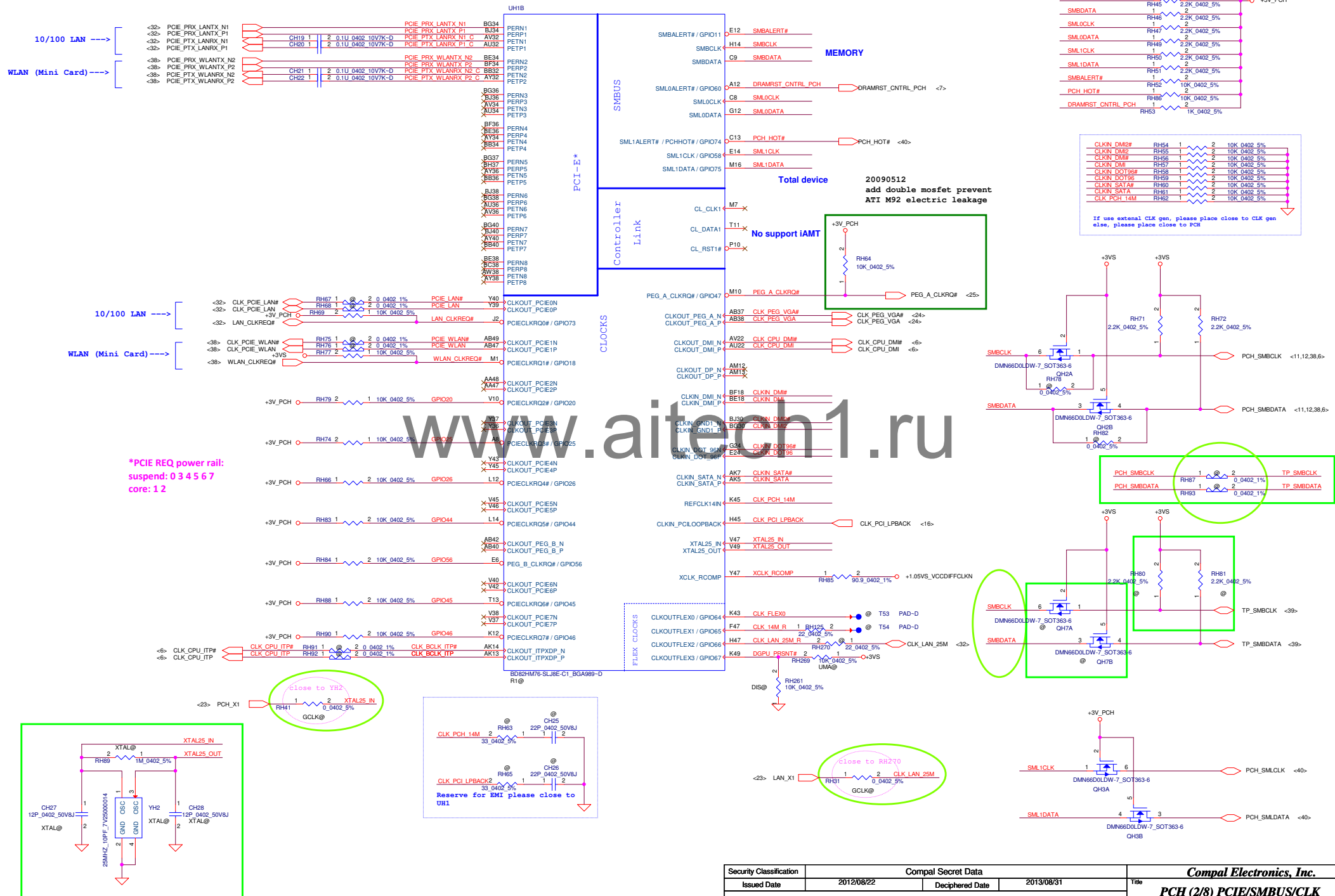
HDA_SDO
ME debug mode, this signal has a weak internal PD
L=>security measures defined in the Flash
Descriptor will be in effect (default)
H=>Flash Descriptor Security will be overridden

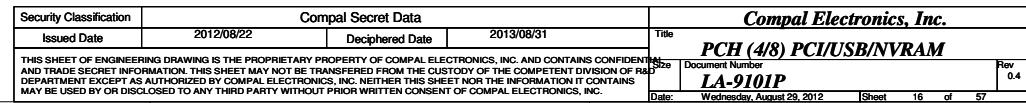
HDA_SYNC
This signal has a weak internal pull-down
On Die PLL VR is supplied by
1.5V when snapied high
1.8V when snapied low
Needs to be pulled High for Huron River platform

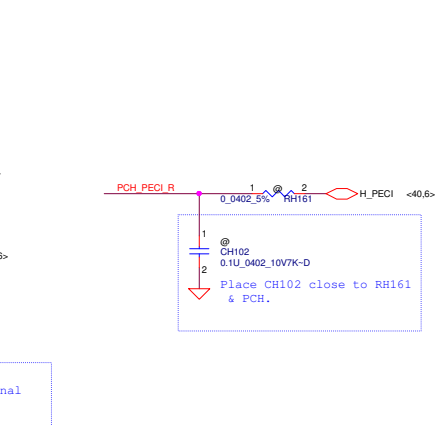
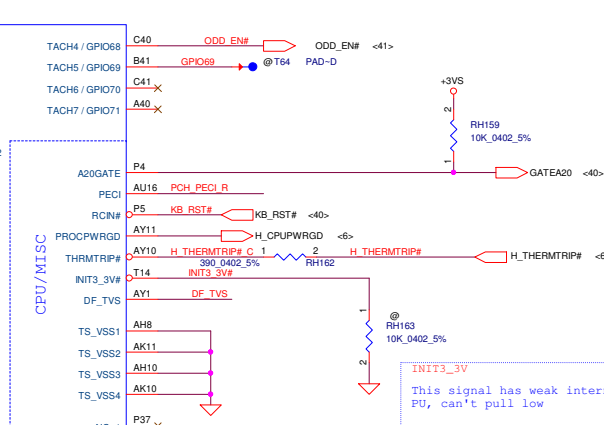
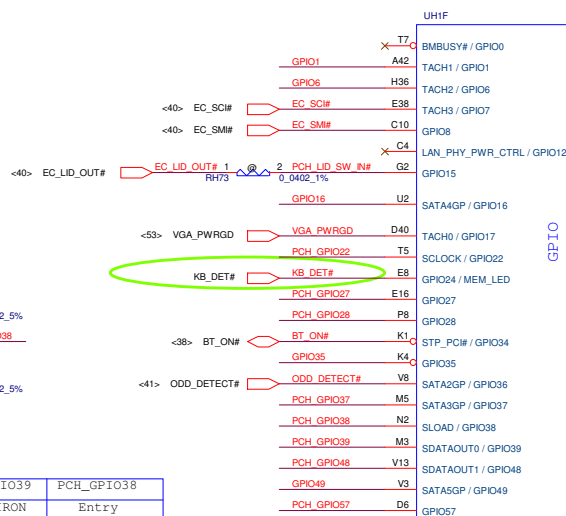
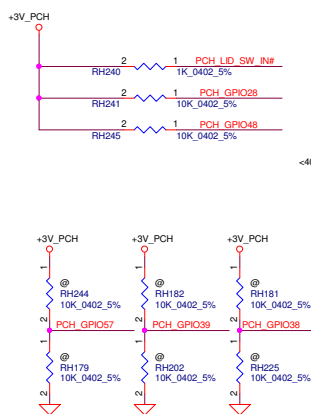
RTC Battery



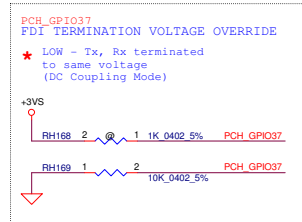
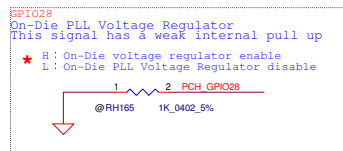
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Issued Date	2012/08/22	Deciphered Date	2013/08/31	PCH (I/8) SATA/HDA/SPI/LPC	
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				LA-9101P	
				Date: Wednesday, August 28, 2012	Sheet 13 of 57



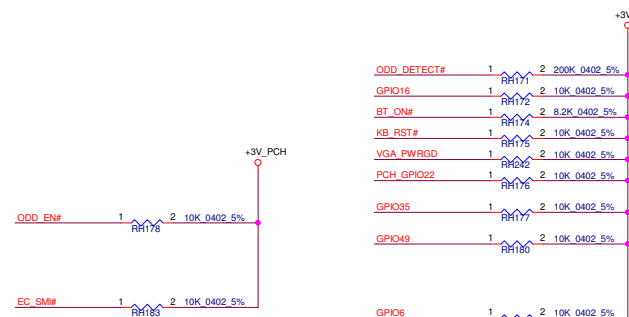
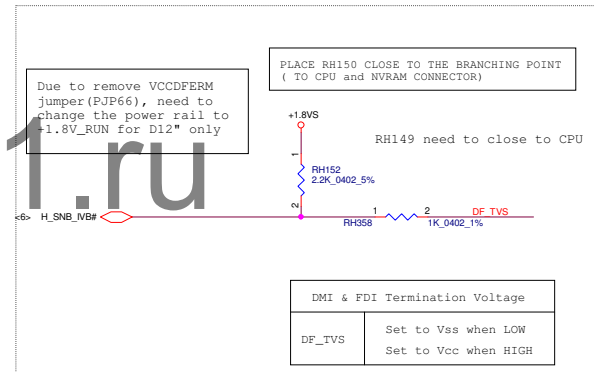


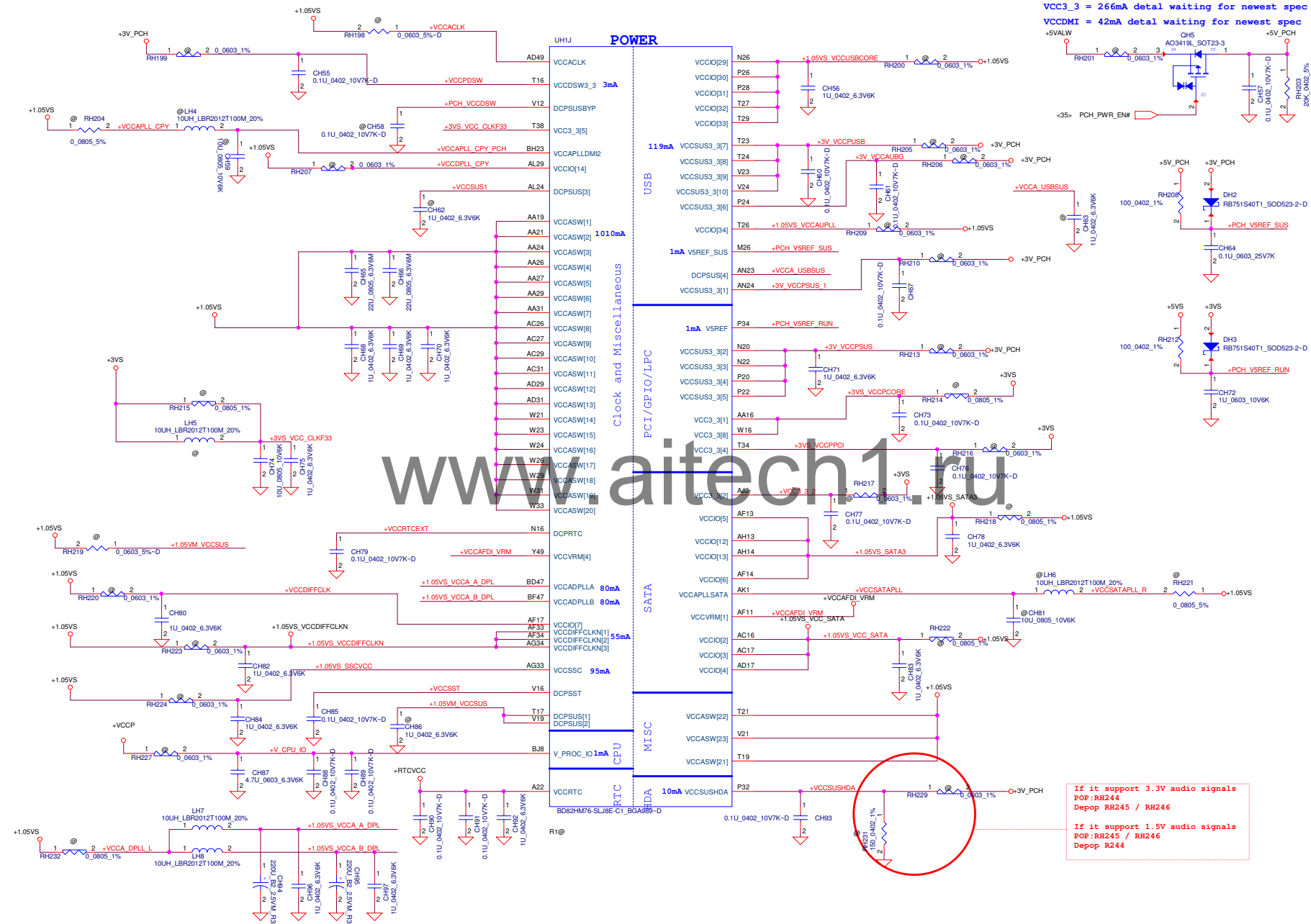


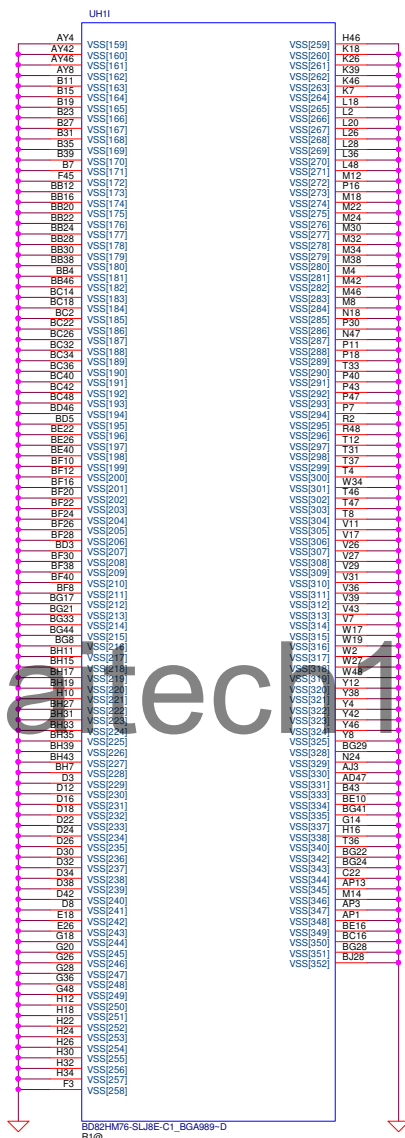
System ID	PCH_GPIO57	PCH_GPIO39	PCH_GPIO38
LOW	VAW00 15''	INSPIRON	Entry
HIGH	VAW10 17''	VOSTRO	Mainstream



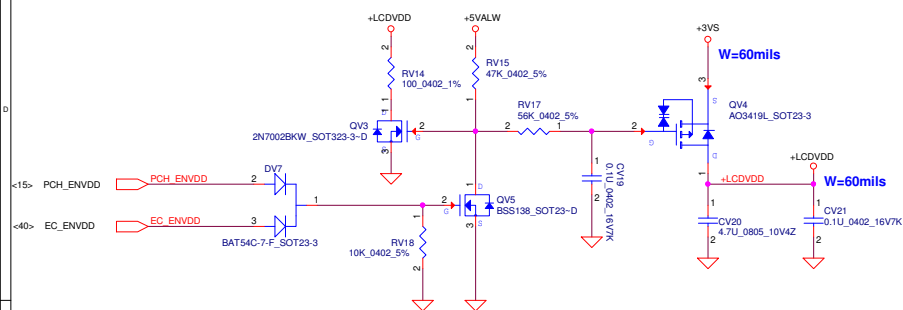
PCH_GPIO28 needs to be connected to XDP_FN8
PCH_GPIO35 needs to be connected to XDP_FN9
PCH_GPIO15 needs to be connected to XDP_FN16
Please refer to Huron River Debug Board DG 0.5



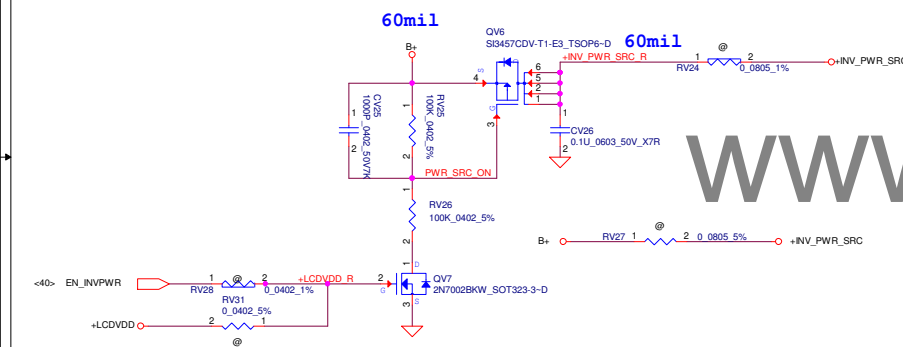




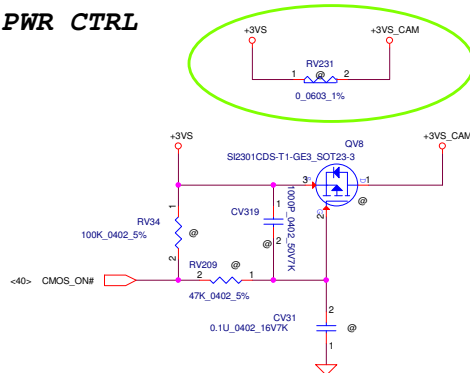
LCD PWR CTRL



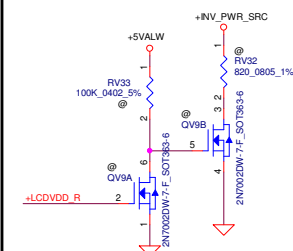
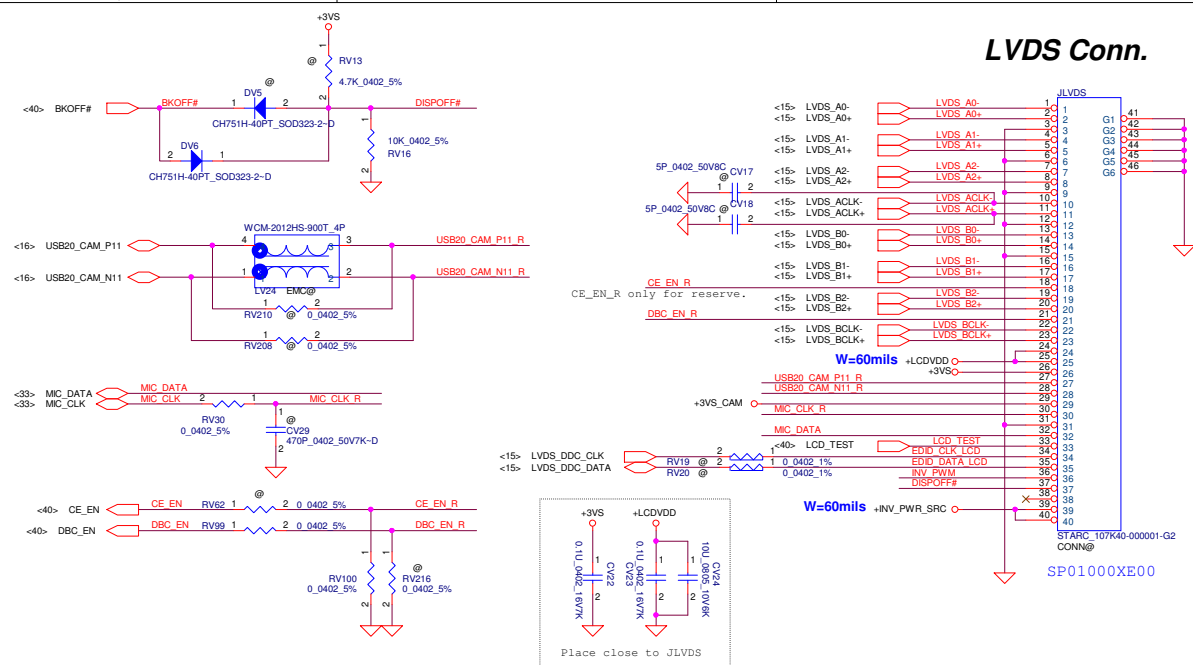
LCD backlight PWR CTRL



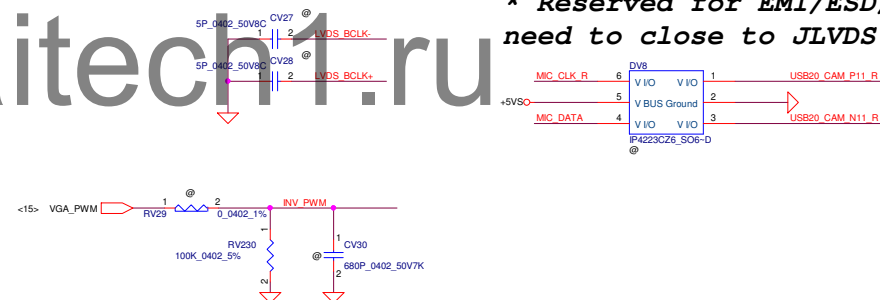
Webcam PWR CTRL



* Reserved for LCD
sequence tuning

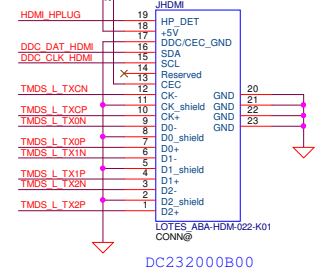
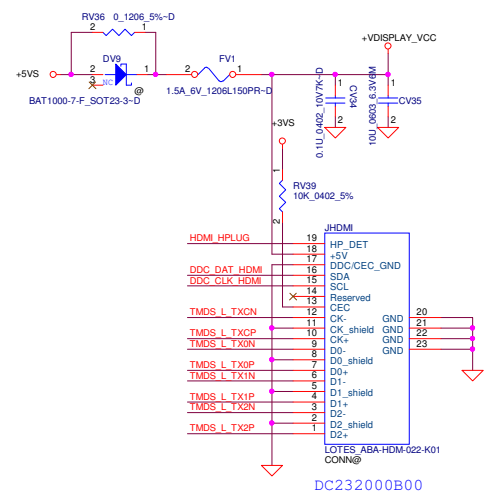
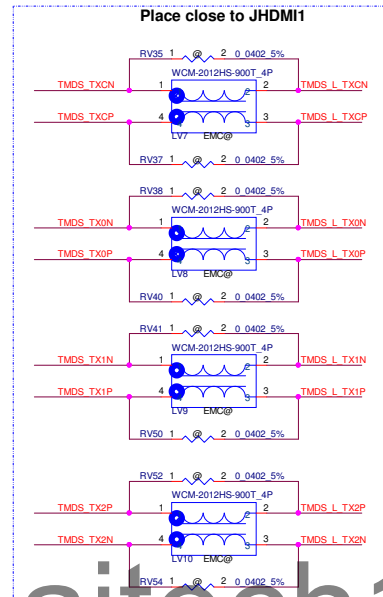
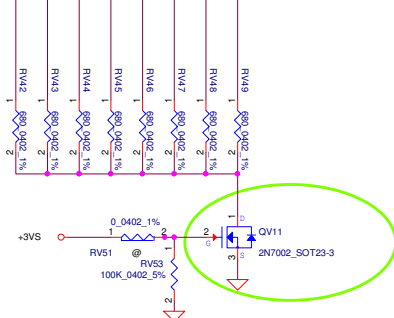
**LVDS Conn.**

* Reserved for EMI/ESD/RF
need to close to JLVDS



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				LA-9101P	0.4
Date	Wednesday August 29, 2012	Sheet	21	of	57

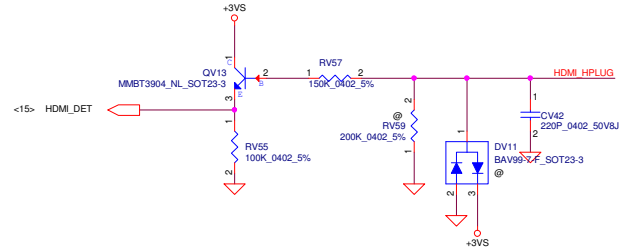
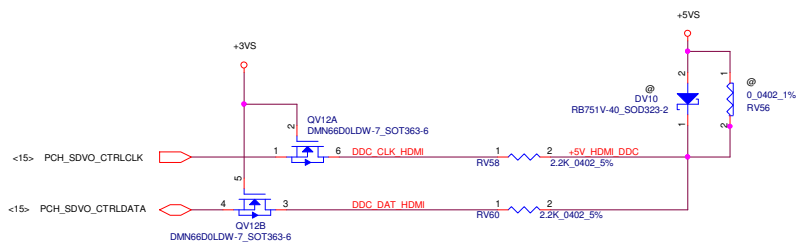
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 <15> HDMI_A2P_VGA CV41 2 1 0.1U 0402 10V7K-D TMD5 TX2P



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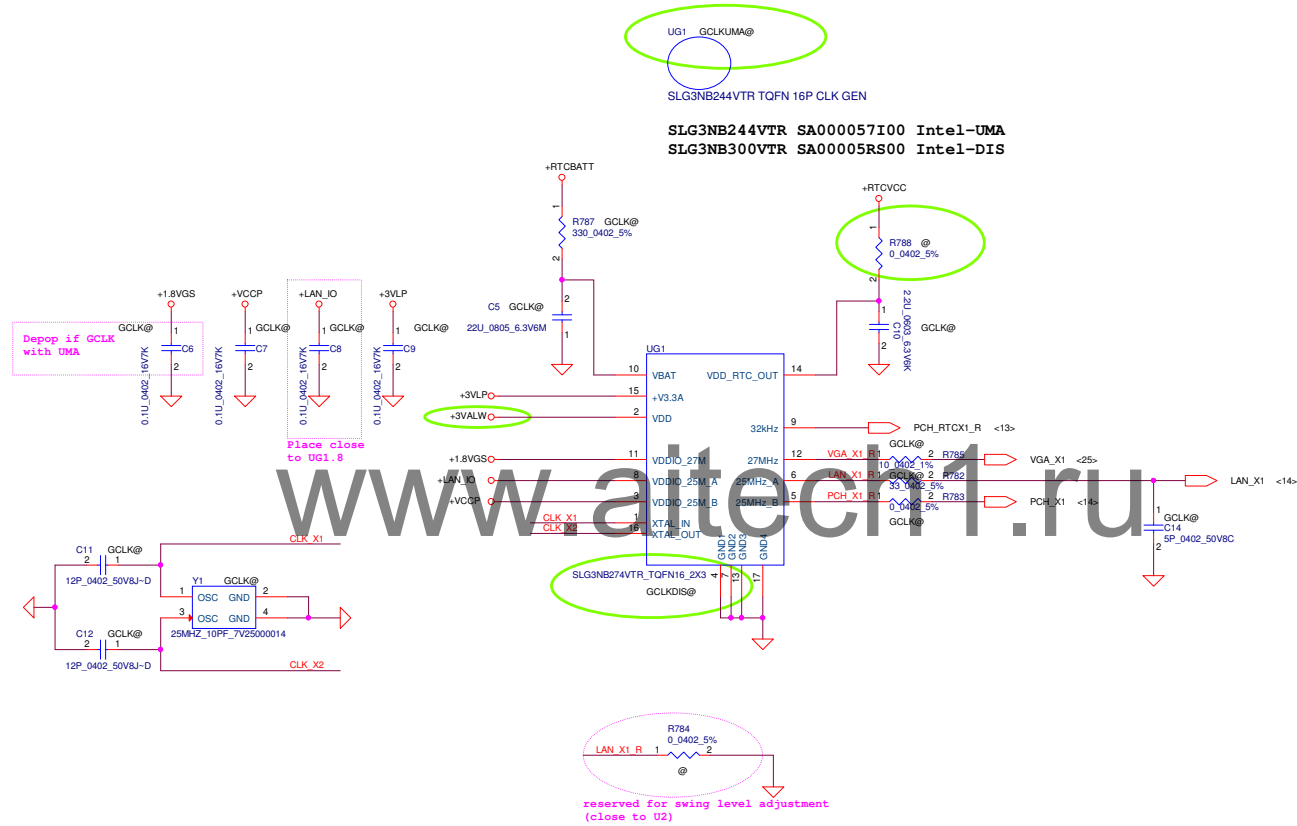
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 TMD5 TX0N @CV362 1 2 100P_0402_50V8J
 TMD5 TX0P @CV363 1 2 100P_0402_50V8J
 TMD5 TX1N @CV359 1 2 100P_0402_50V8J
 TMD5 TX1P @CV357 1 2 100P_0402_50V8J
 TMD5 TX2N @CV361 1 2 100P_0402_50V8J
 TMD5 TX2P @CV364 1 2 100P_0402_50V8J

TMD5 L TXCN CV349 1 2 3.3P_0402_50V8C-D
 TMD5 L TXCP CV350 1 2 3.3P_0402_50V8C-D
 TMD5 L TX0N CV351 1 2 3.3P_0402_50V8C-D
 TMD5 L TX0P CV352 1 2 3.3P_0402_50V8C-D
 TMD5 L TX1N CV353 1 2 3.3P_0402_50V8C-D
 TMD5 L TX1P CV354 1 2 3.3P_0402_50V8C-D
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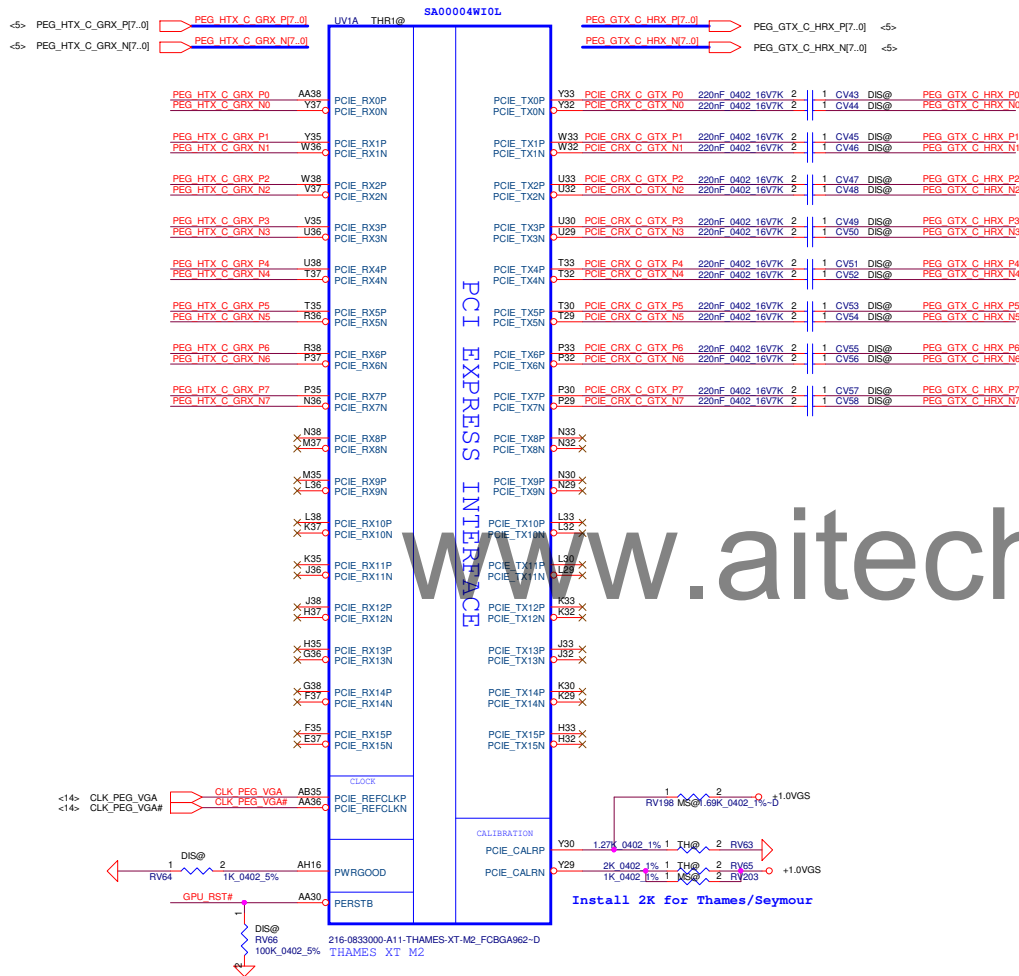


Part Number	Description
8000000023M	HDMI W/Logo:8000000023M

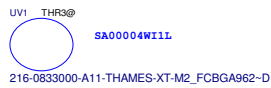
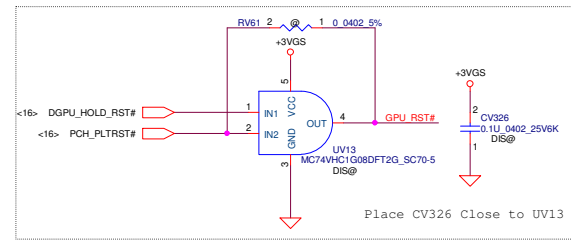
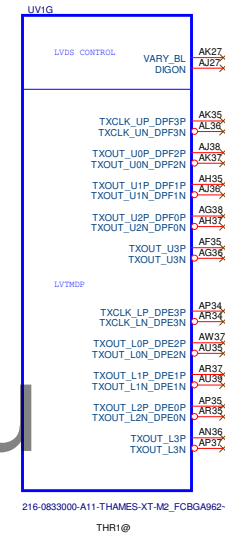
Security Classification	2012/08/22	Deciphered Date	2013/08/31	Title	HDMI
Issued Date	2012/08/22	Deciphered Date	2013/08/31	Document Number	LA-9101P
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Date: Wednesday, August 28, 2012					Sheet 22 of 57



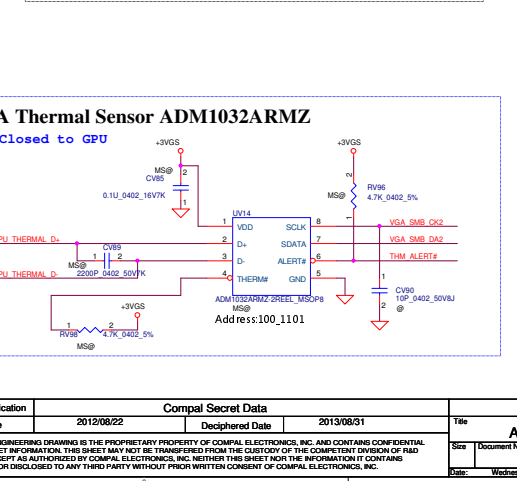
GFX PCIE LANE REVERSAL



LVDS Interface



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Issued Date	2012/08/22	Deciphered Date	2013/08/31	ATI ThamesXT M2 PCIE/LVDS	
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				Date	Wednesday, August 28, 2012
				Sheet	24 of 57

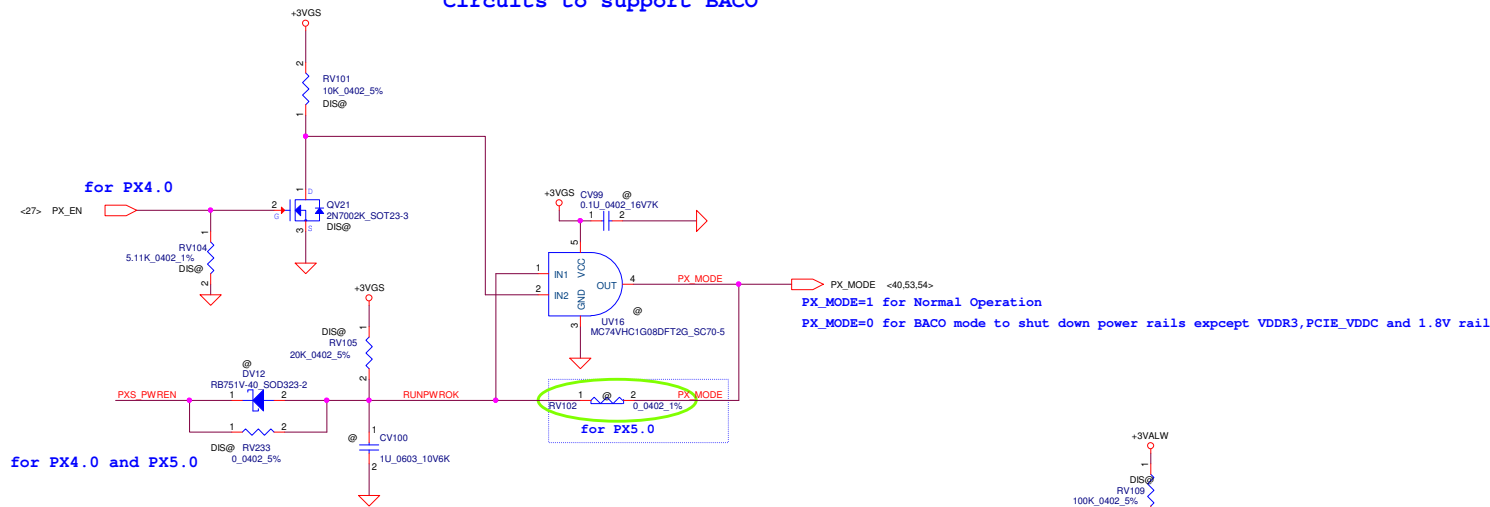


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Issued Date	2010/08/22		Deciphered Date		2010/08/31		AT1 ThamesXT M2 Main MSC		
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							LA-9101P		
							Date:	Wednesday, August 25, 2012	

Switch circuits in BACO desings for Thanos/Seymour only

55mA@1.0V, in BACO mode

Circuits to support BACO



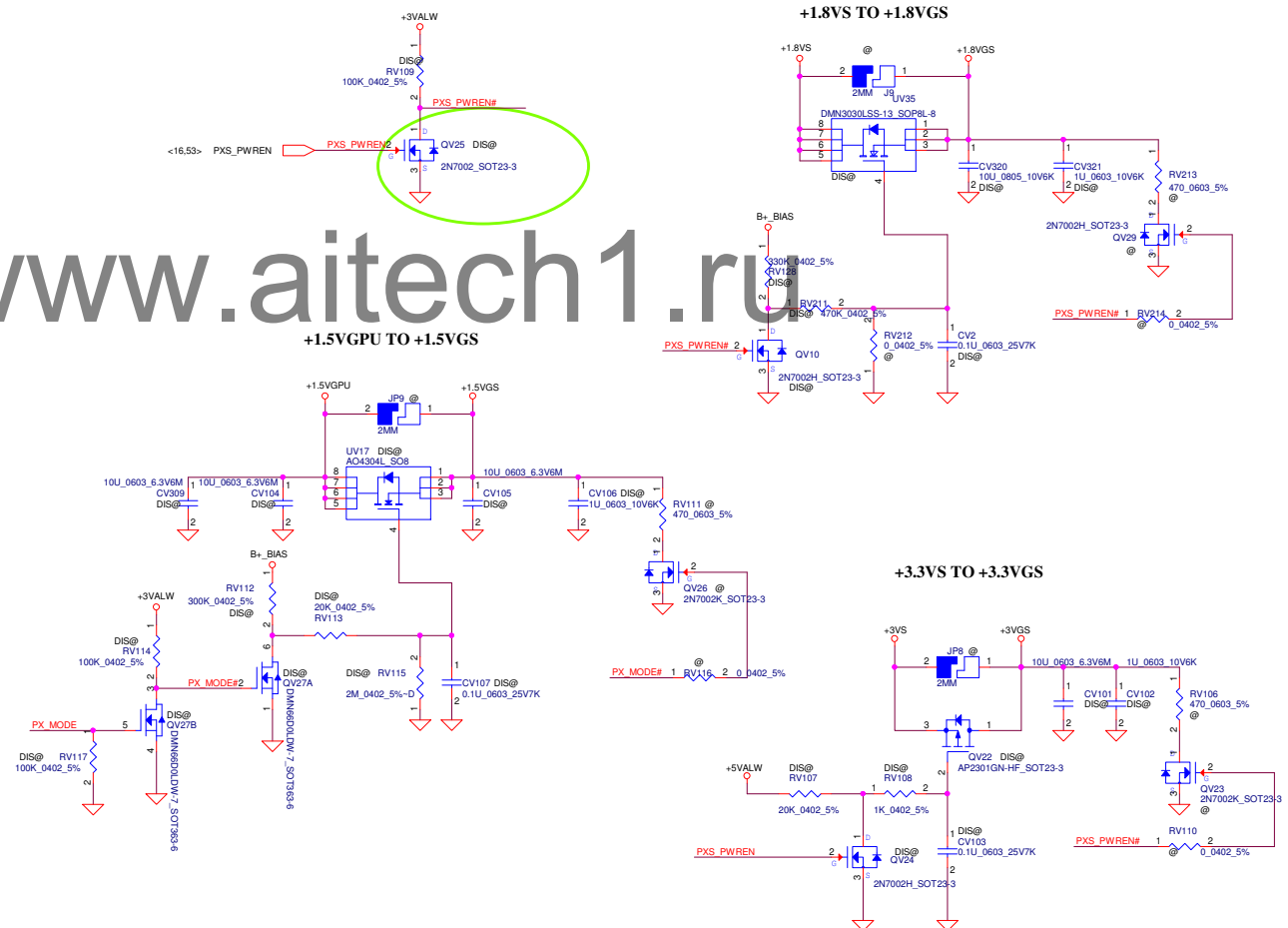
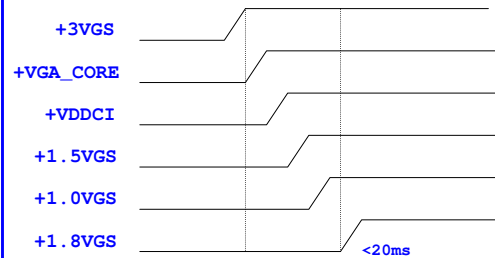
Note:

PX4.0 +VGA_CORE, VDDCI, +1.5VGS ON

PX4.0 +3VGS, +1.0VGS, +1.8VGS OFF

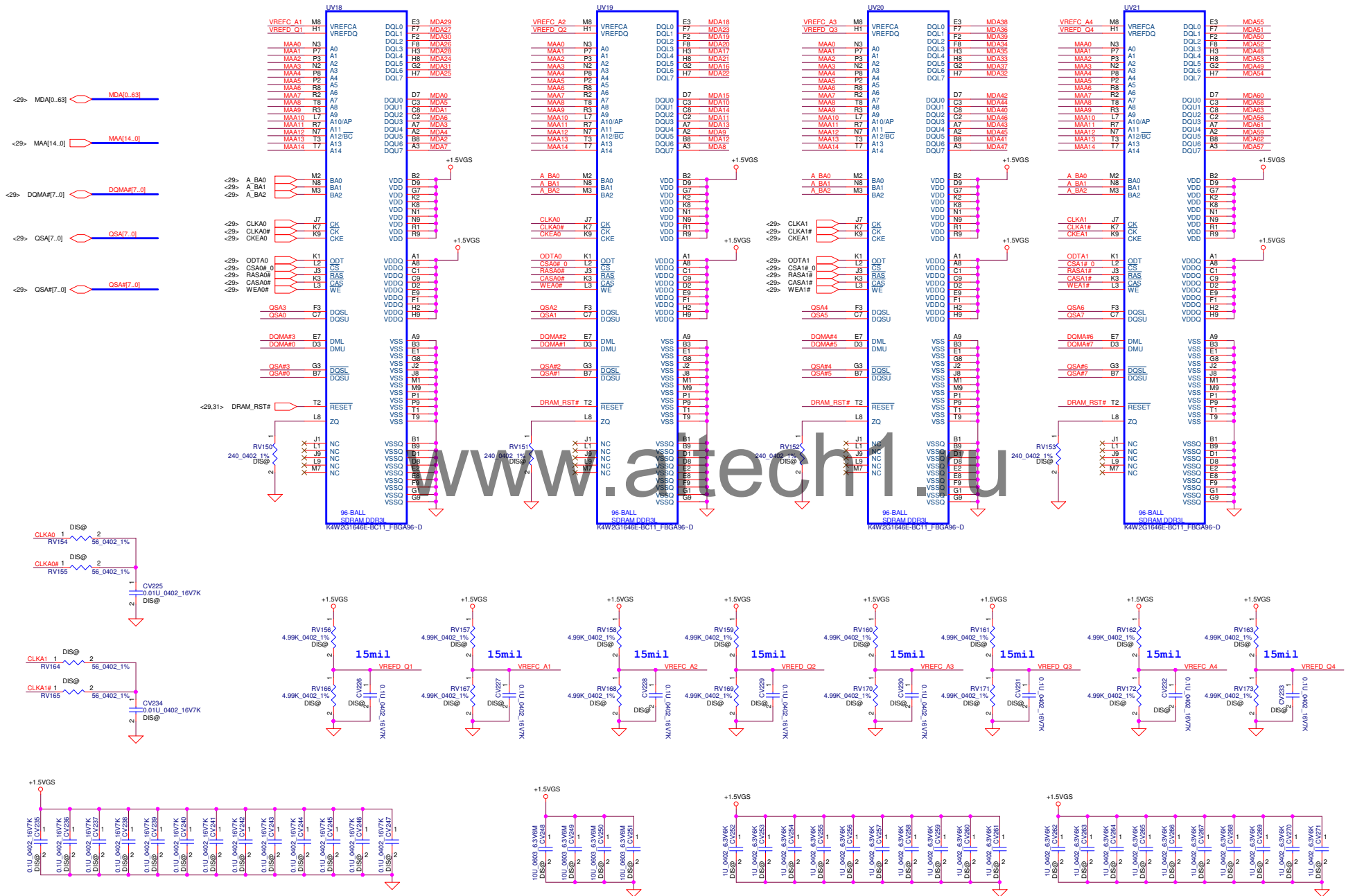
PX5.0 +3VGS, +VGA_CORE, VDDCI, +1.5VGV, +1.0VGS, +1.8VGS OFF

Power Sequence of Thames and Mars Pro



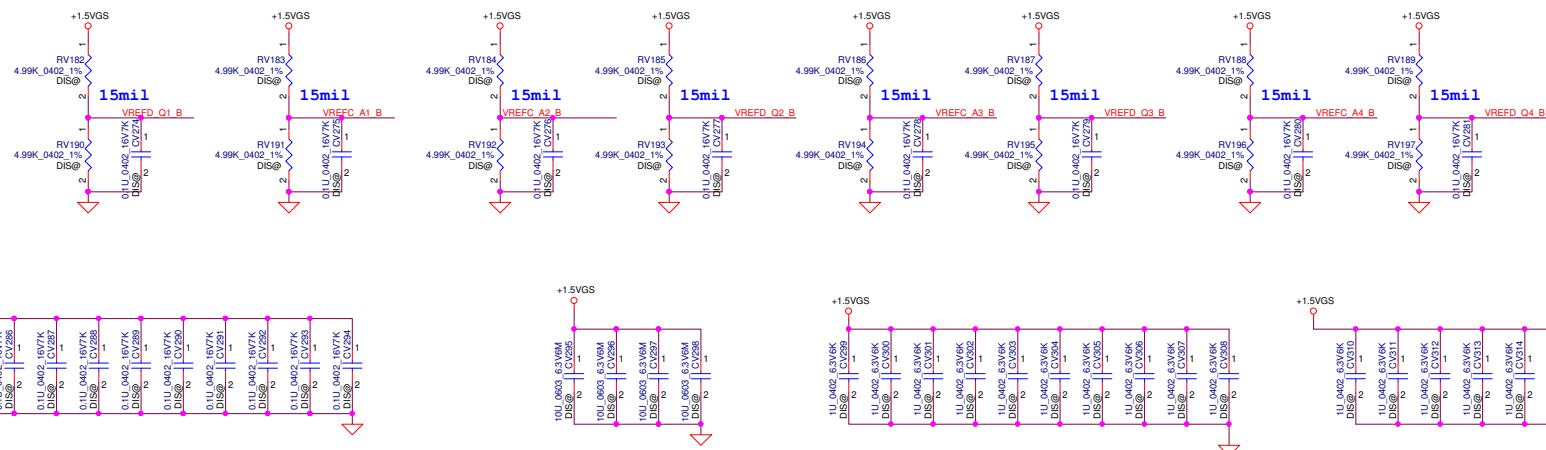
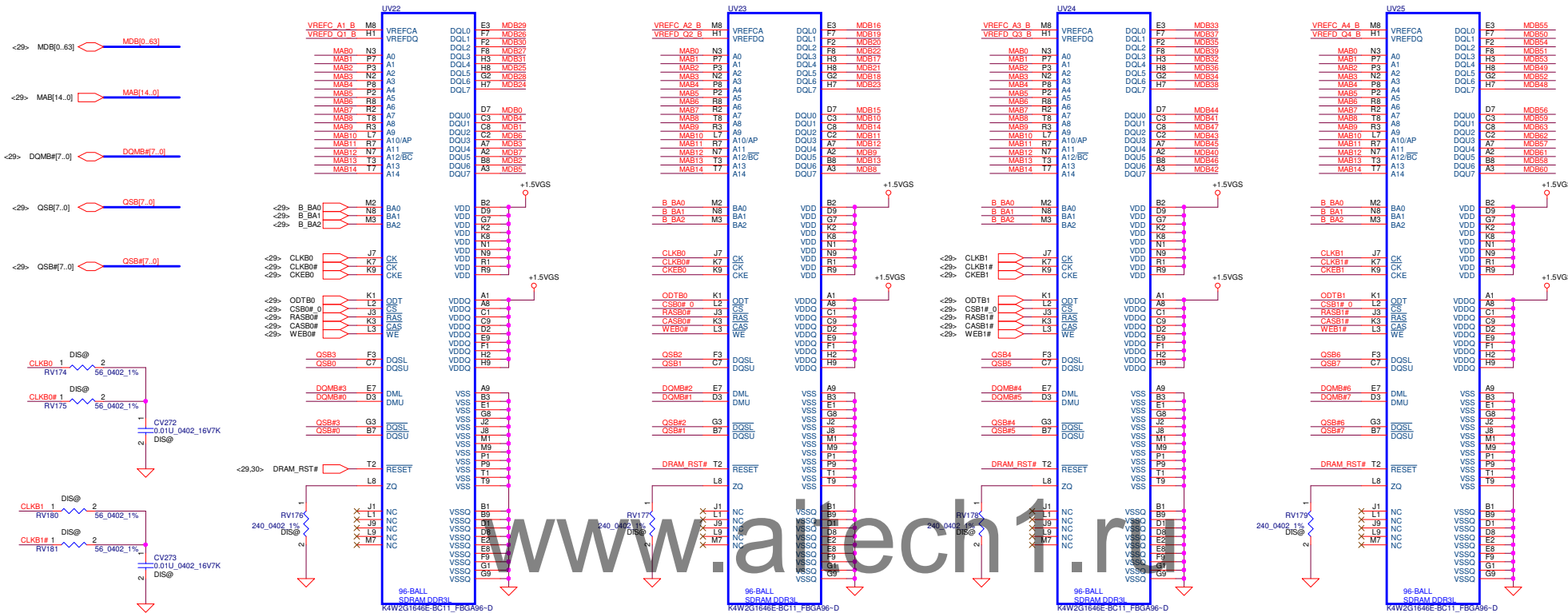
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					LA-9101P	
Date:	Wednesday, August 29, 2012		Sheet	26 of 57		

CHANNEL A: 256MB/512MB DDR3

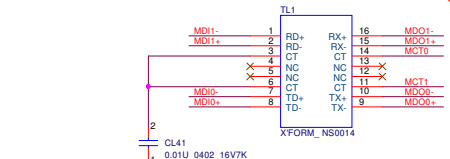
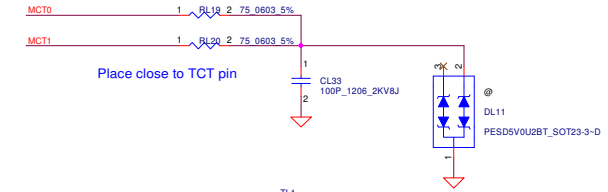
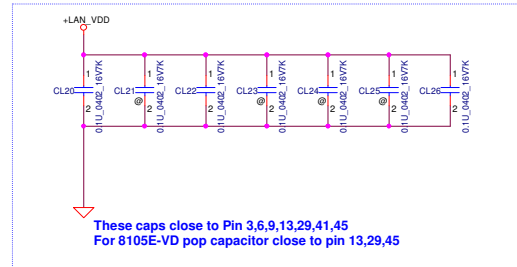
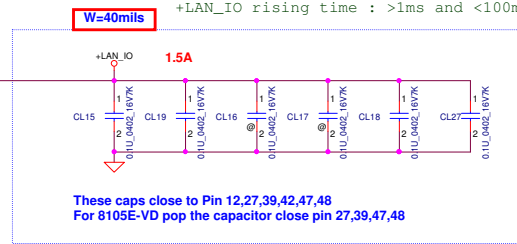
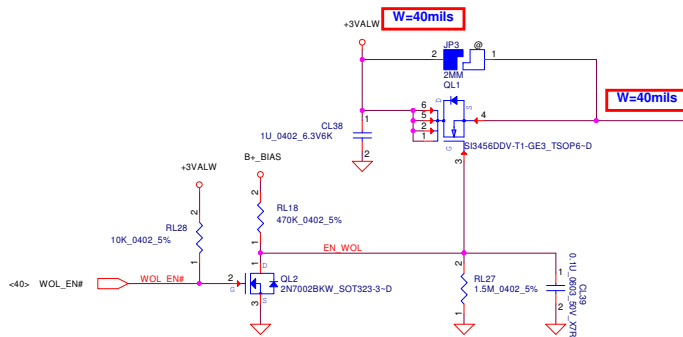


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					ATI ThamesXT M2 VRAM_A
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					LA-9101P
					Rev 0.4
Date:		Wednesday, August 29, 2012		Sheet	30 of 57

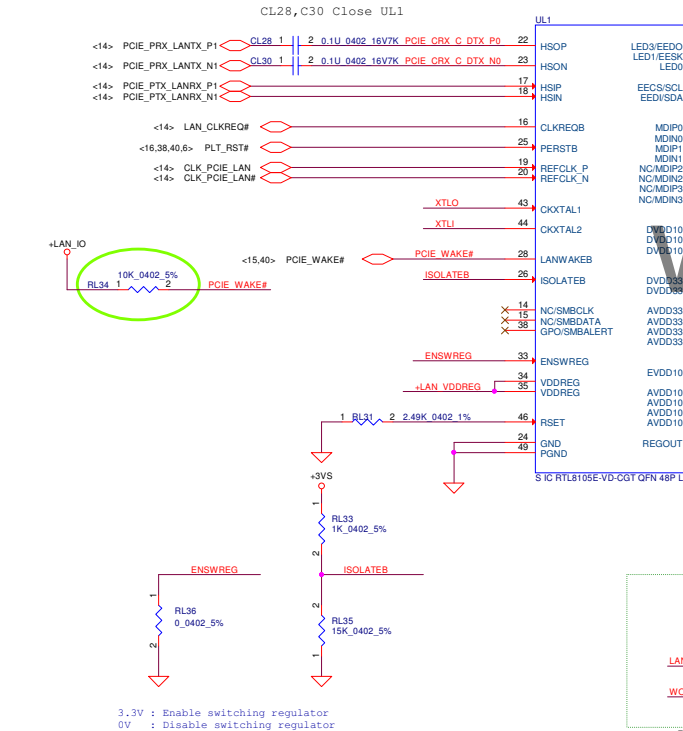
CHANNEL B: 256MB/512MB DDR3



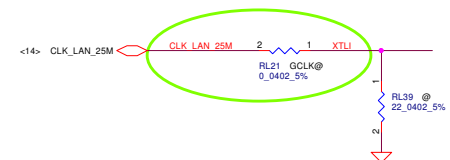
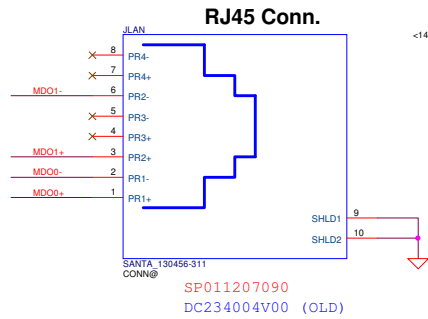
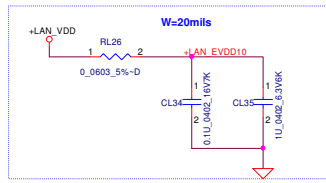
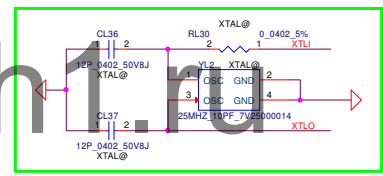
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					Size	Document Number	Rev
					LA-9101P		0.4
Date:	Wednesday, August 29, 2012	Sheet	31	of	57		



DL11 as close as possible to C27 and C32

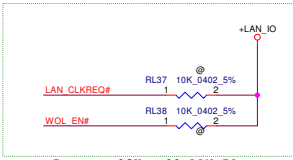


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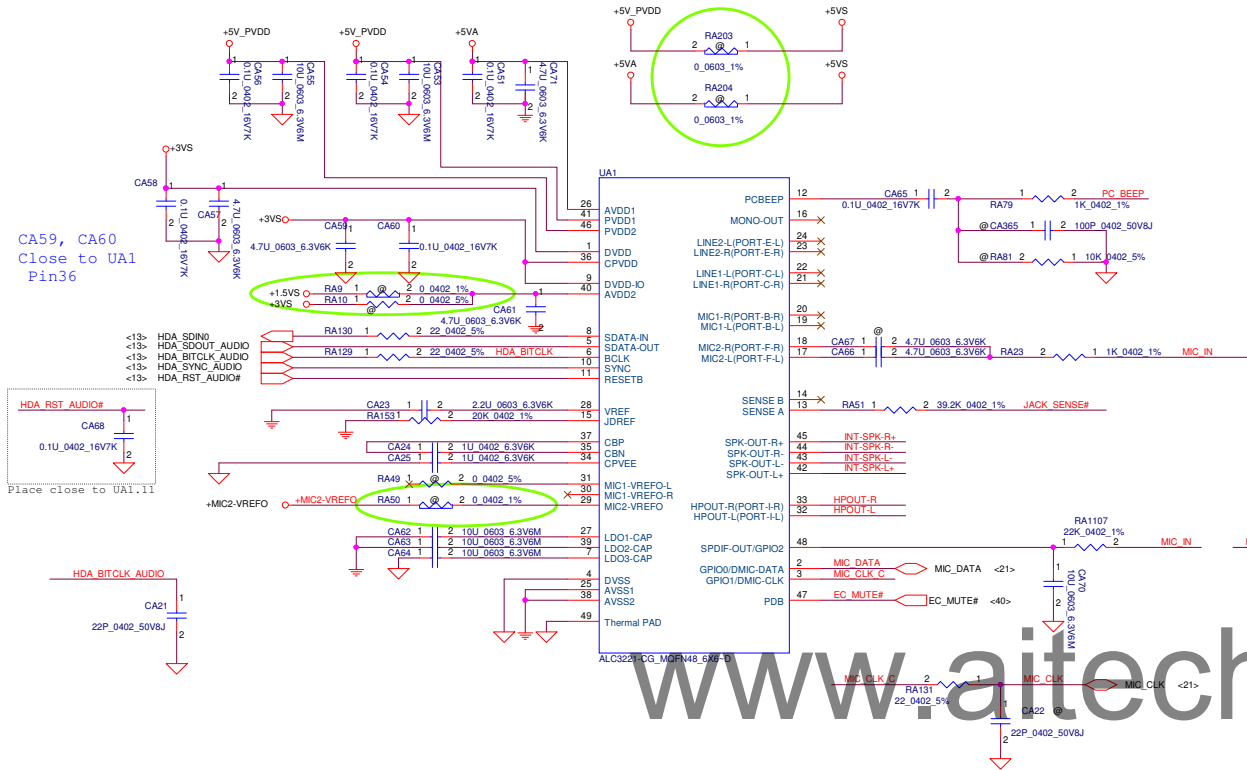
3.3V : Enable switching regulator
0V : Disable switching regulator

10/100 : 100@ (LDO mode used)

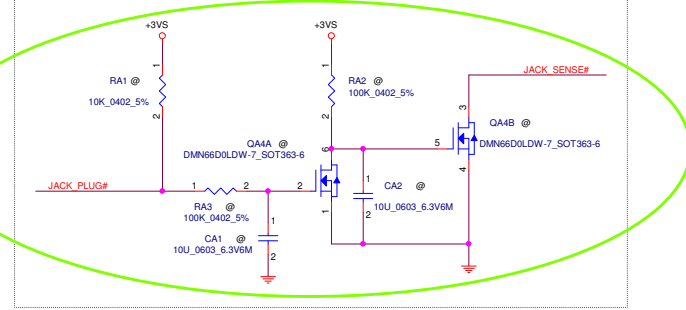


Reserve 10K pull LAN_IO

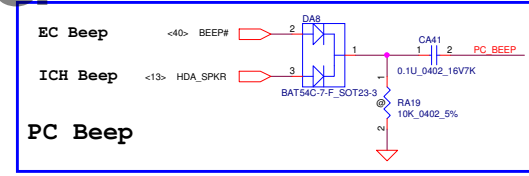
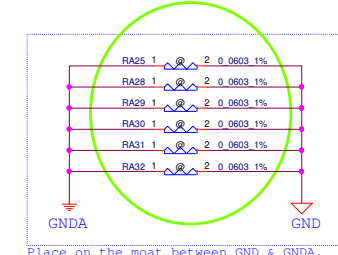
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					LA-9101P
				Date	Wednesday, August 23, 2012
				Sheet	32 of 57



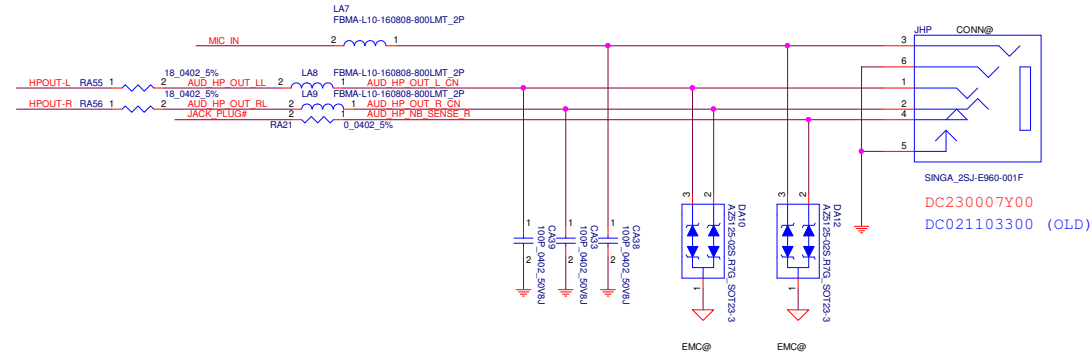
JACK_PLUG Delay circuitis



Reserve for cancel Delay circuitis

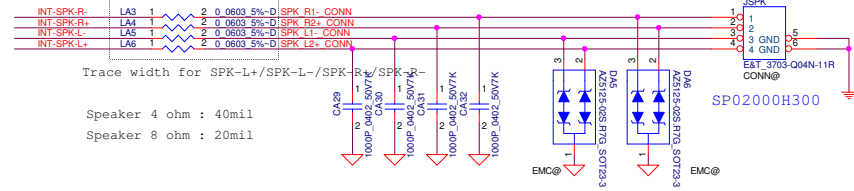


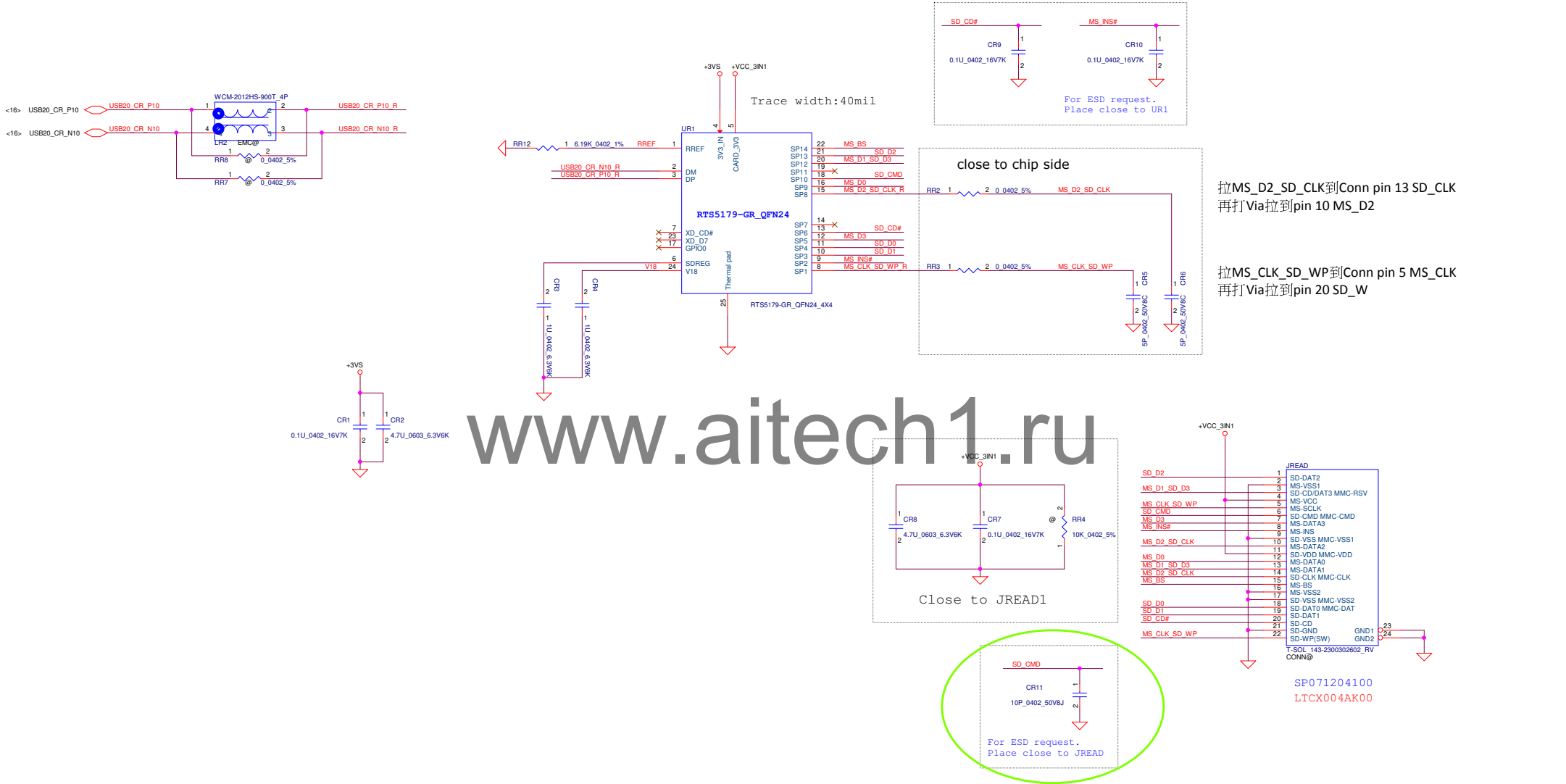
iPhone type Combo Jack



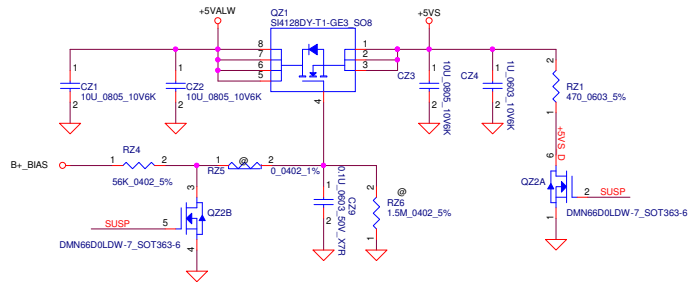
Close to UA1
Pin11,13,14,16

close to Codec

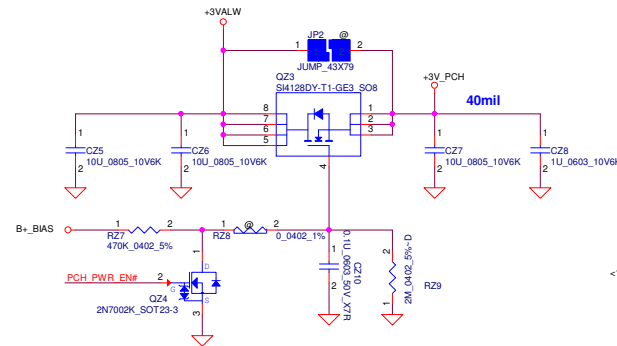




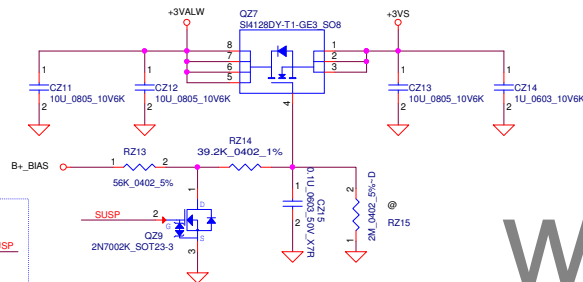
+5VALW to +5VS



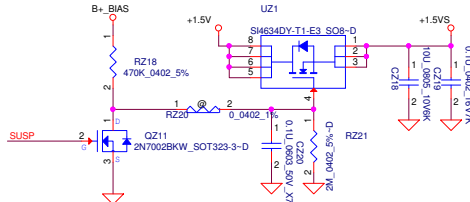
+3VALW to +3V_PCH



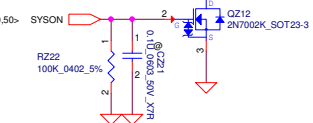
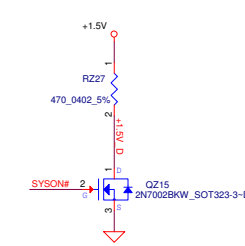
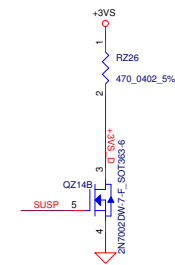
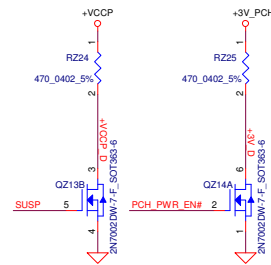
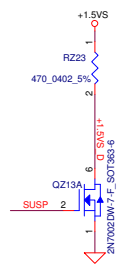
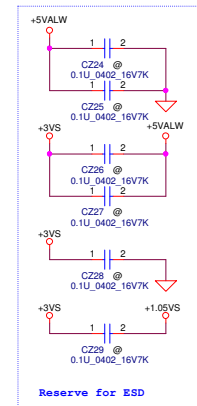
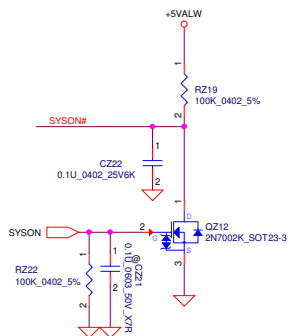
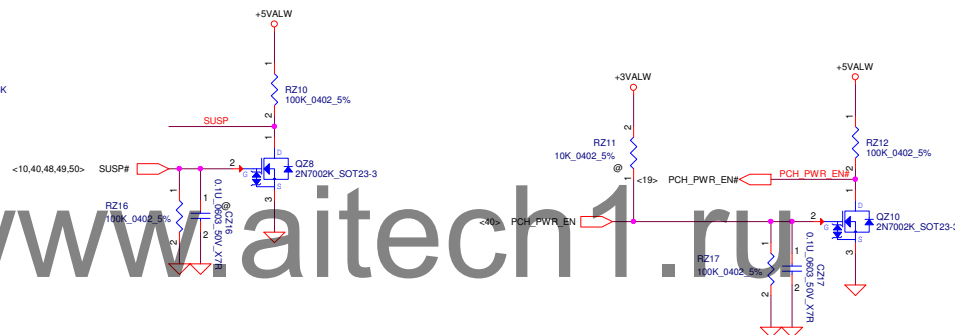
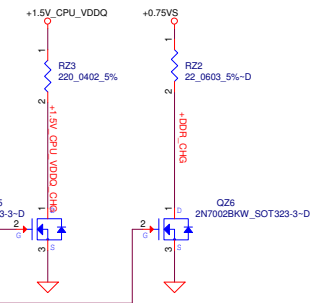
+3VALW to +3VS



+1.5V To +1.5VS

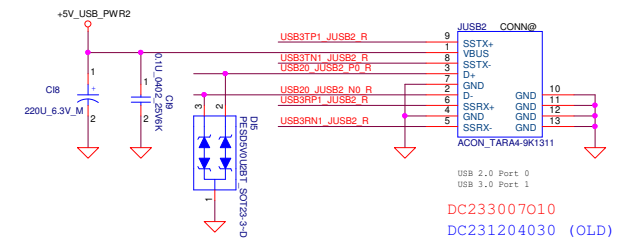
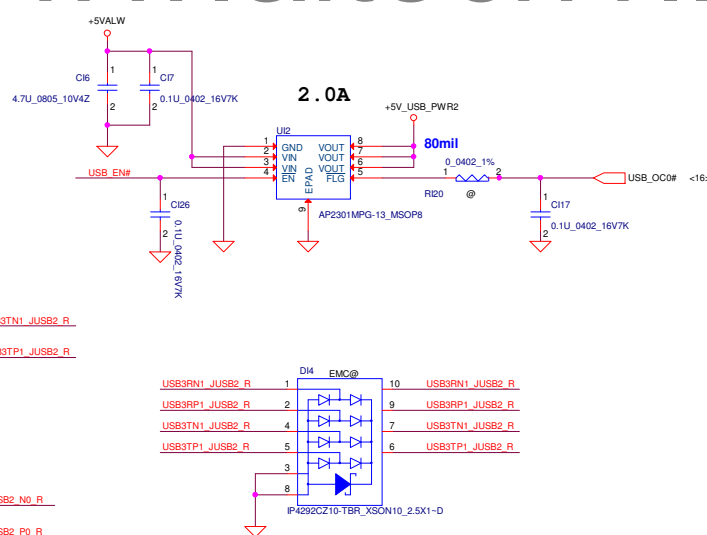
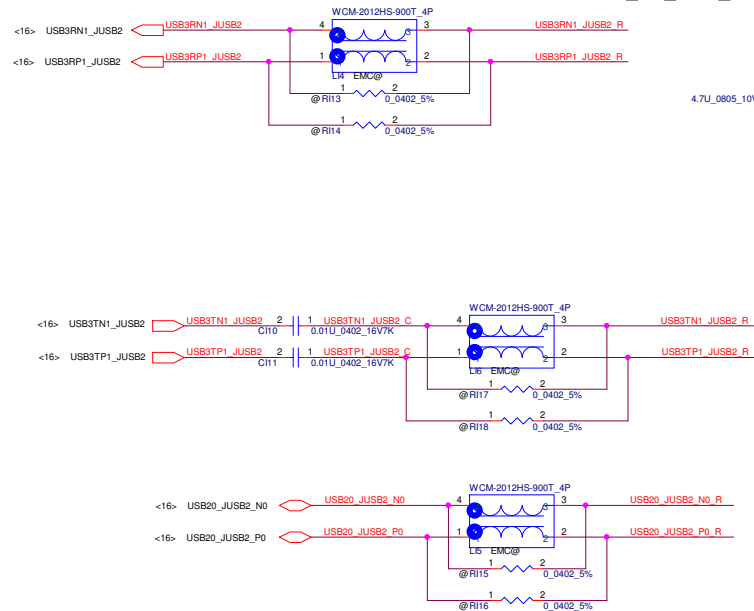
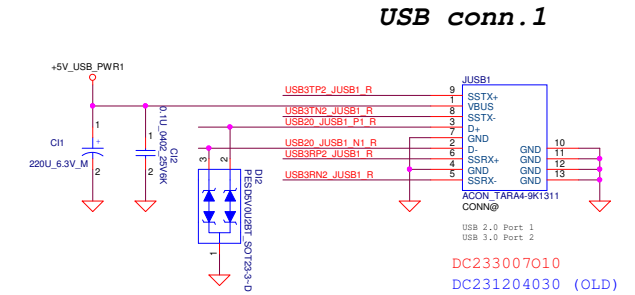
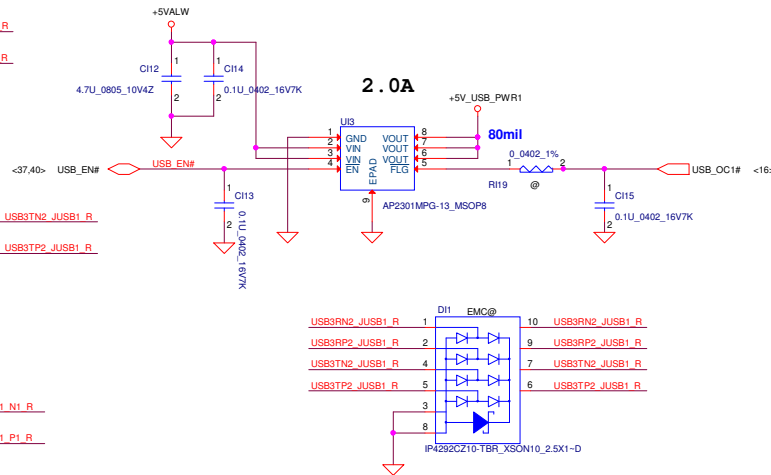
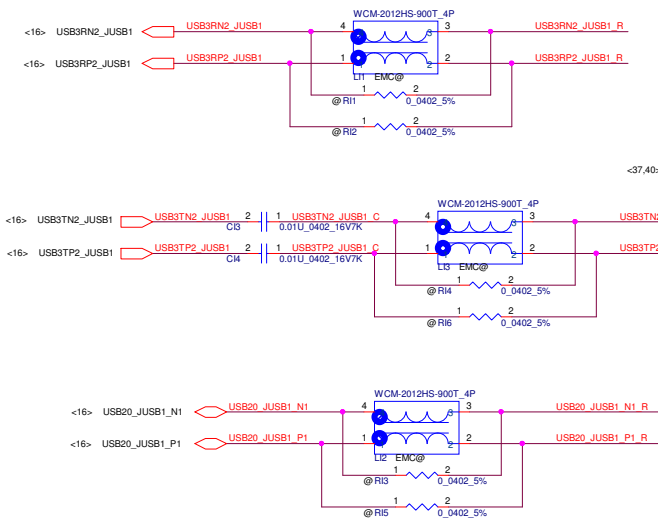


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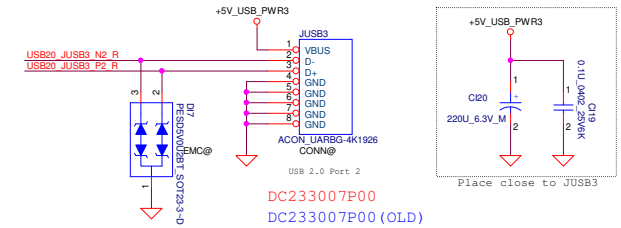
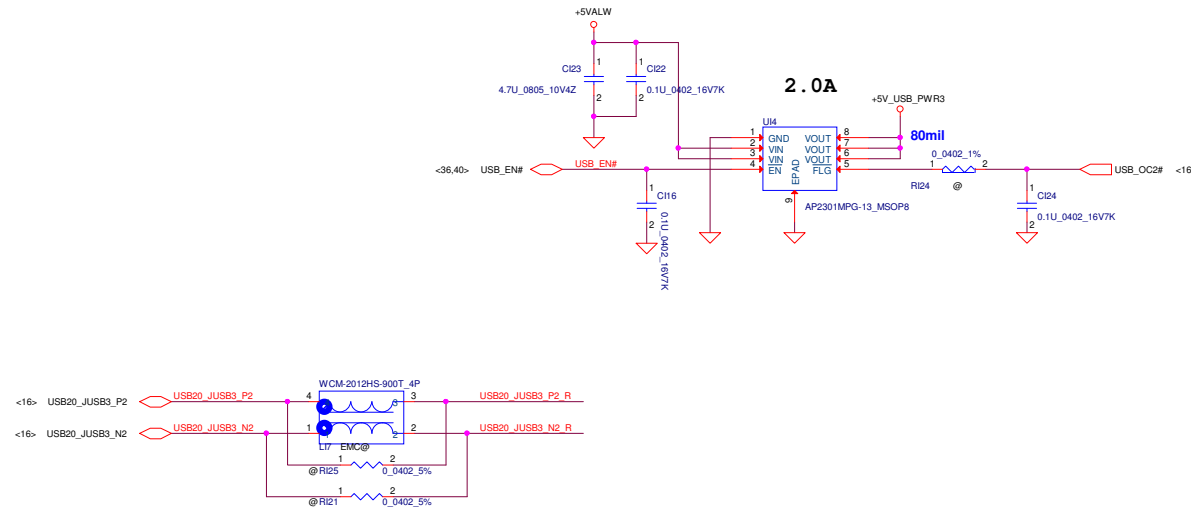


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								Rev 0.4	
								LA-9101P	
								Date: Wednesday, August 28, 2012	
								Sheet 35 of 57	

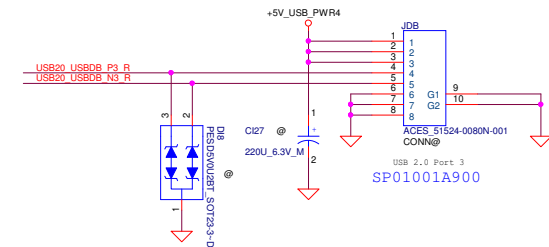
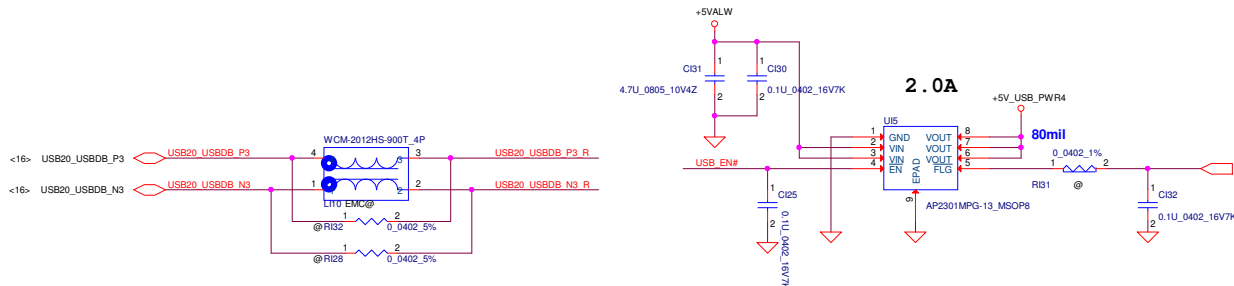
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				0.4	
Date: Wednesday, August 28, 2012				Sheet	36 of 57

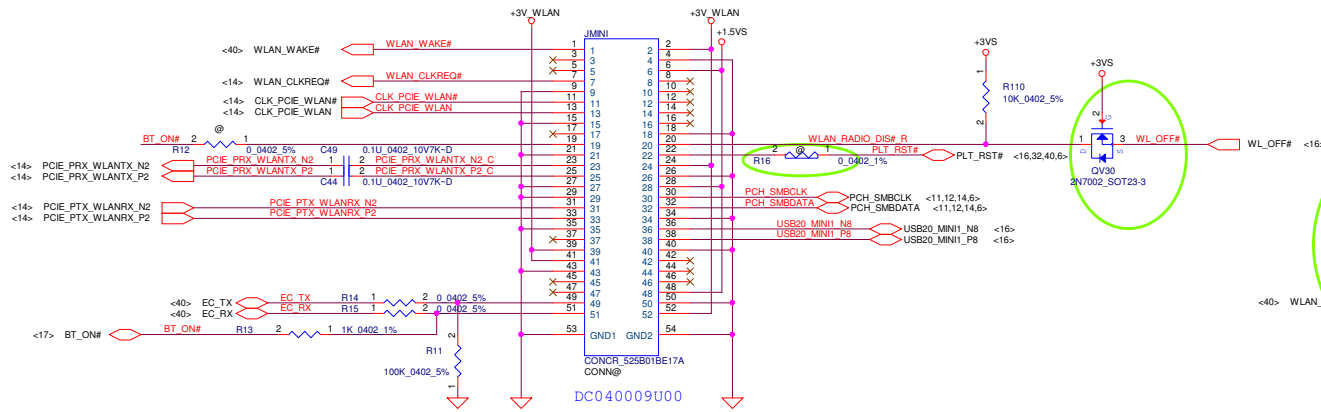


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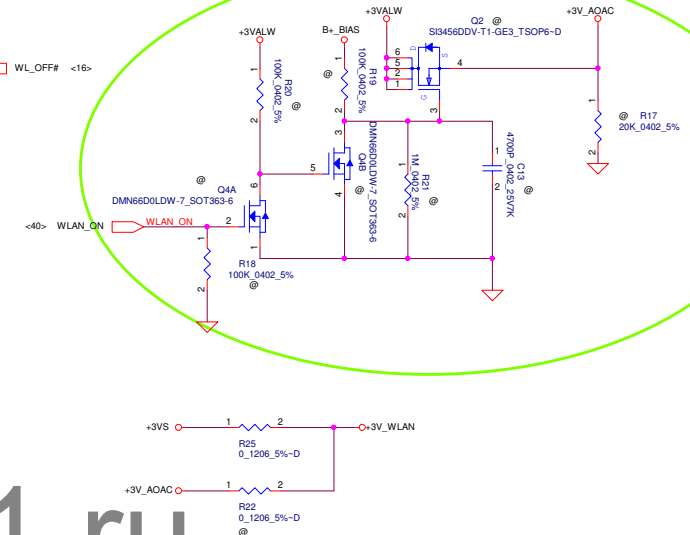


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				Sheet 37 of 57	

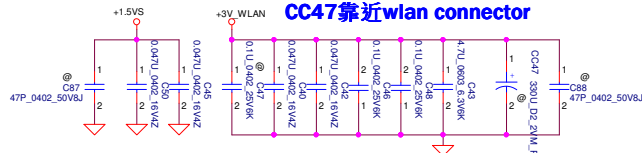
Mini WLAN/WIMAX H=6.7



Power Control for Mini card



CC47靠近wlan connector

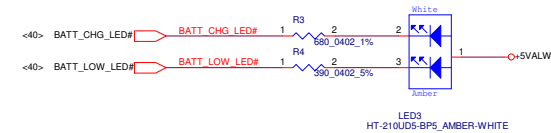


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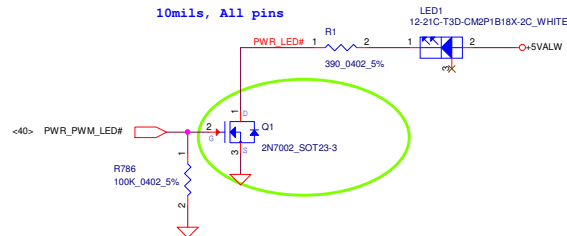
HDD LED



Battery LED



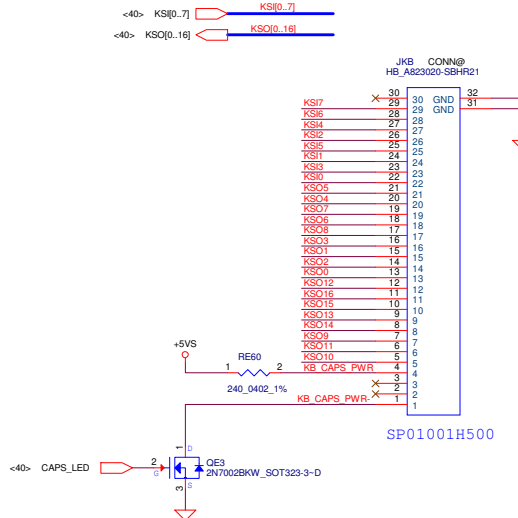
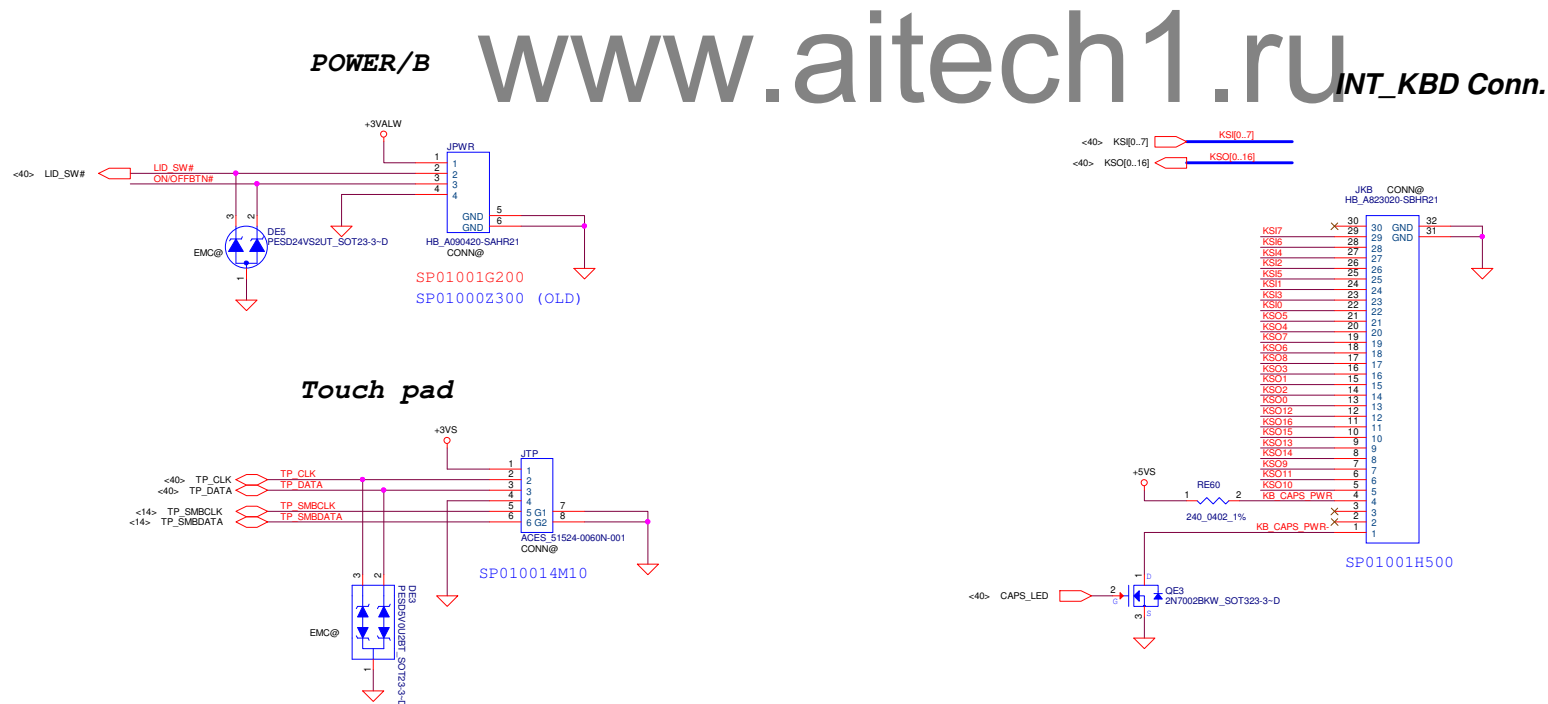
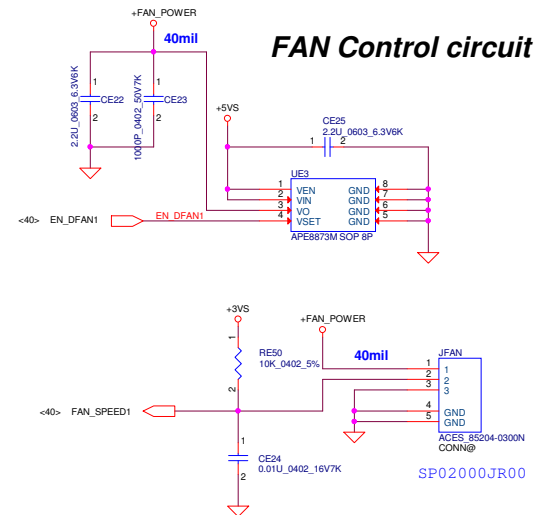
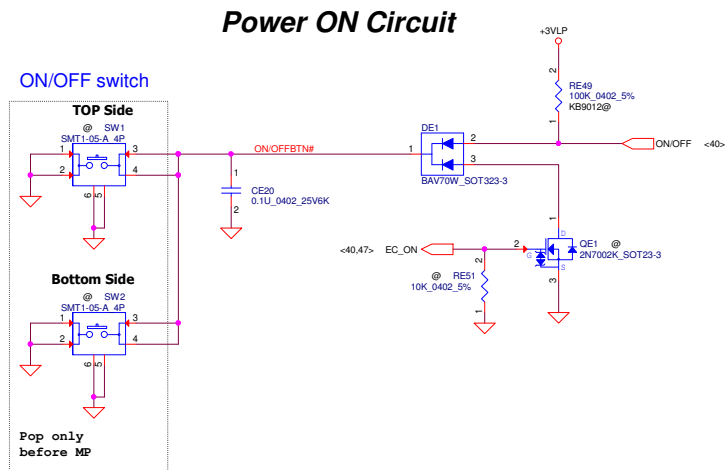
Power LED



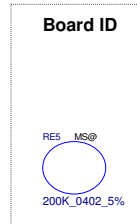
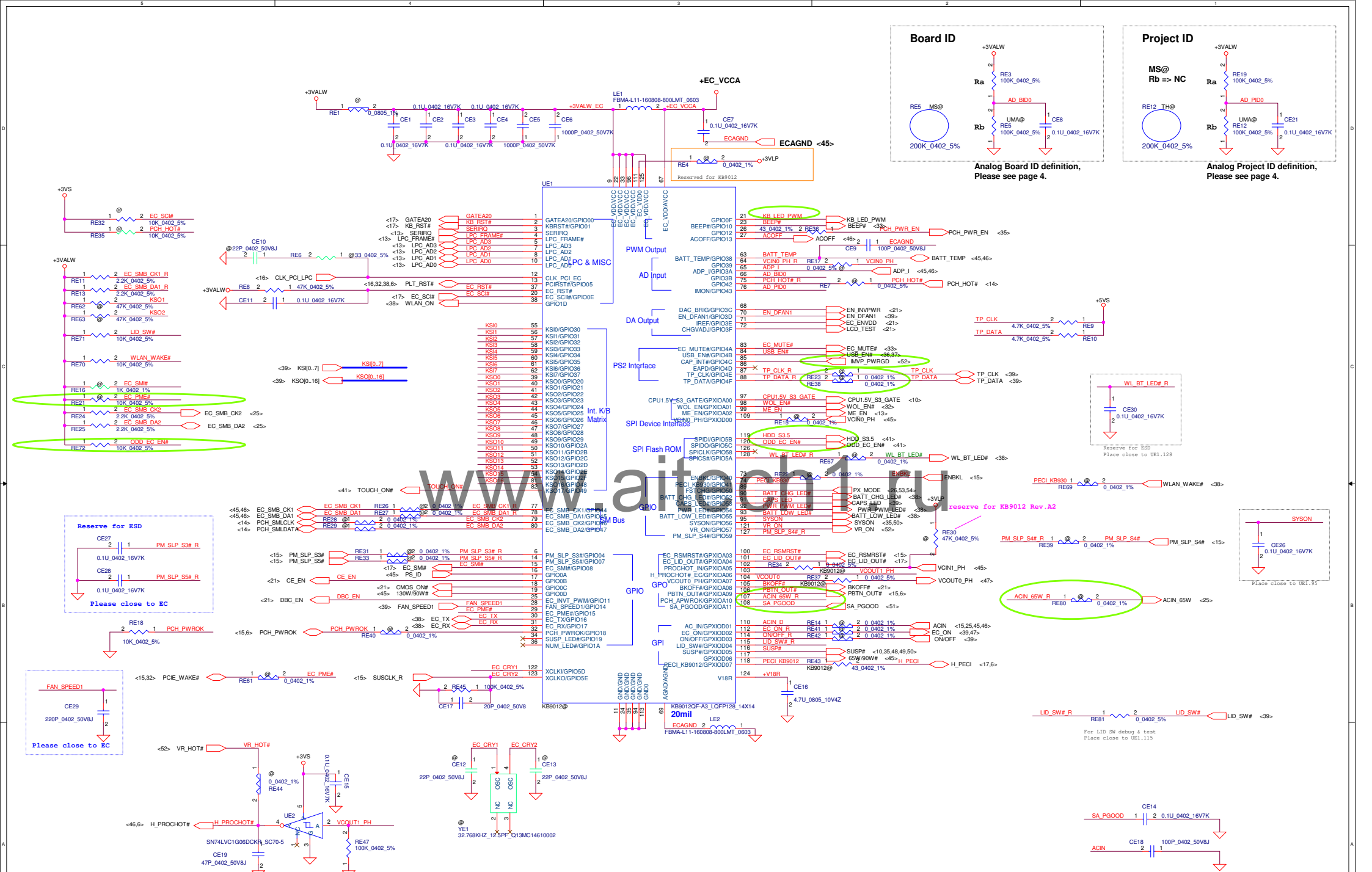
Wireless LED



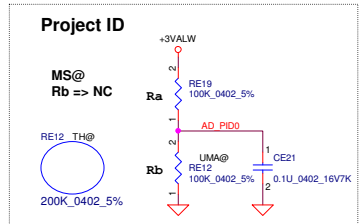
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				Date: Wednesday, August 29, 2012	
				Sheet 38 of 57	



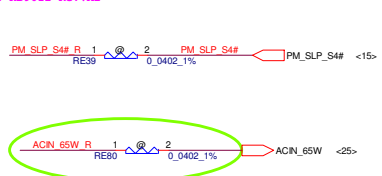
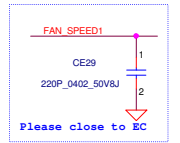
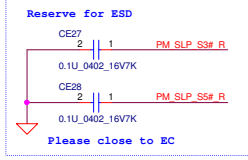
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				LA-9101P	0.4
				Date: Wednesday, August 28, 2012	Sheet 39 of 57



Analog Board ID definition, Please see page 4.



Analog Project ID definition, Please see page 4.

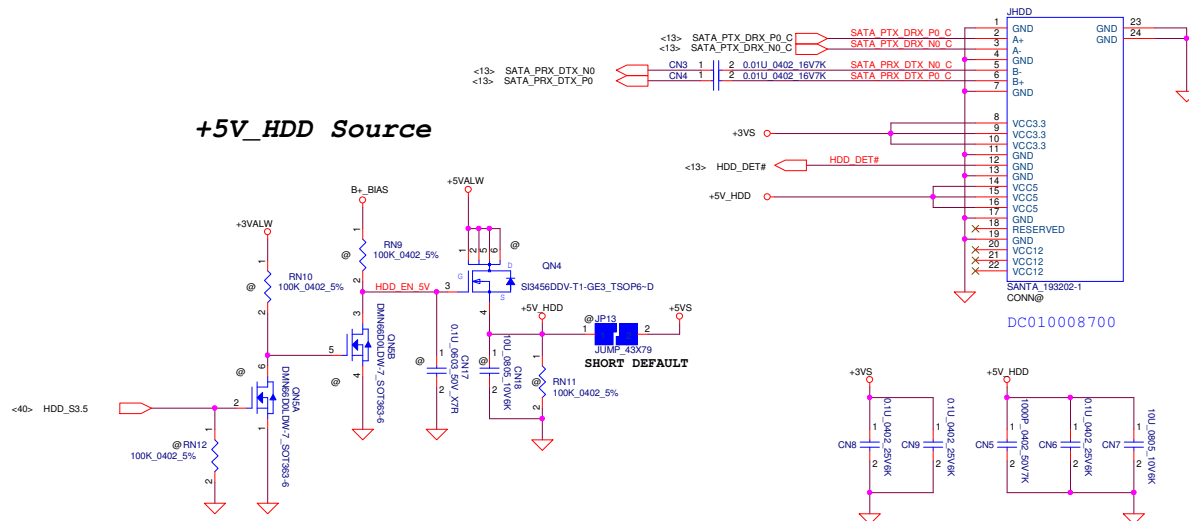


For LID SW debug & test Place close to UE1.115

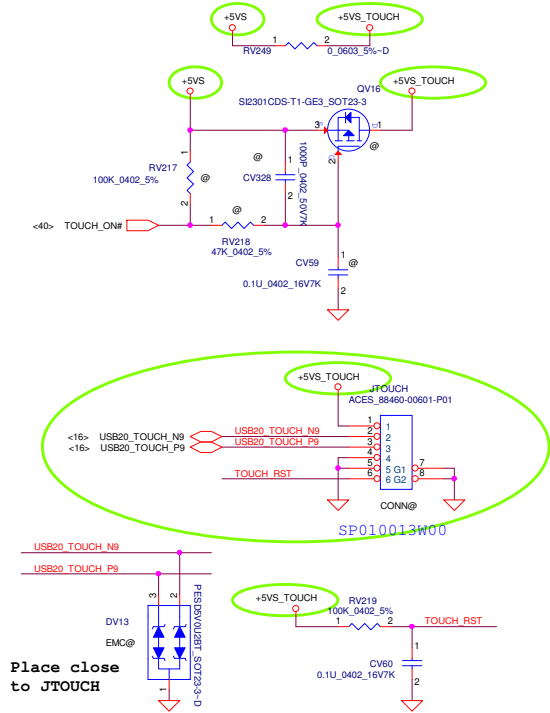
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2012/08/22		2013/08/31		LA-9101P	
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2012/08/22		2013/08/31		Wednesday, August 28, 2012	
40		40		Sheet	
40		40		of 57	

SATA HDD Conn.

+5V_HDD Source

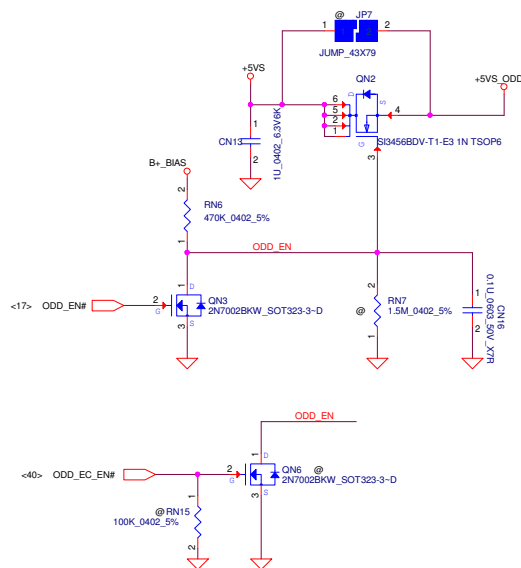


* Touch Screen Panel

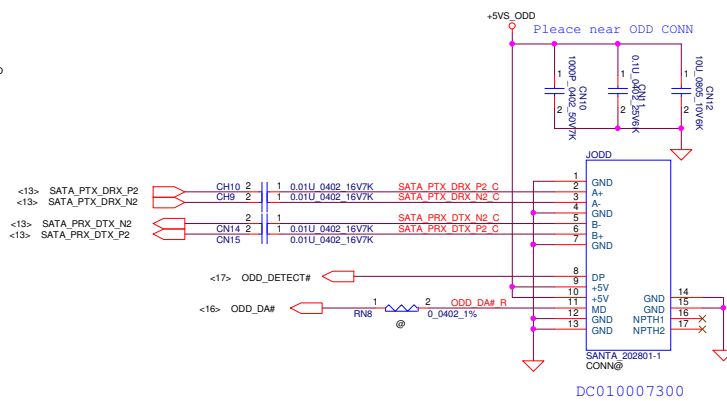


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ODD Power Control

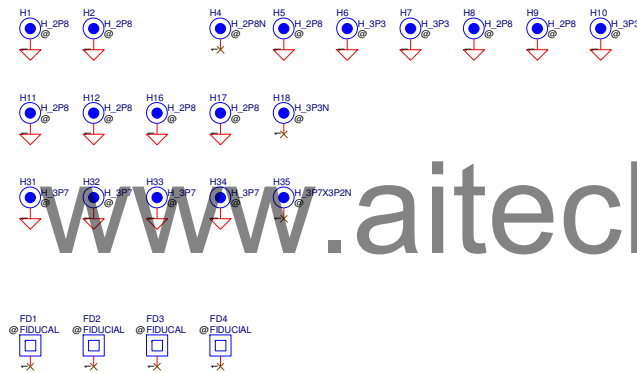


SATA ODD Conn.



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LA-9101P				41	0.4
Date: Wednesday, August 28, 2012				Sheet	of 57

Screw Hole



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Date: Wednesday, August 28, 2012		Sheet 42 of 57		0.4	

Version Change List (P. I. R. List)

Page 1

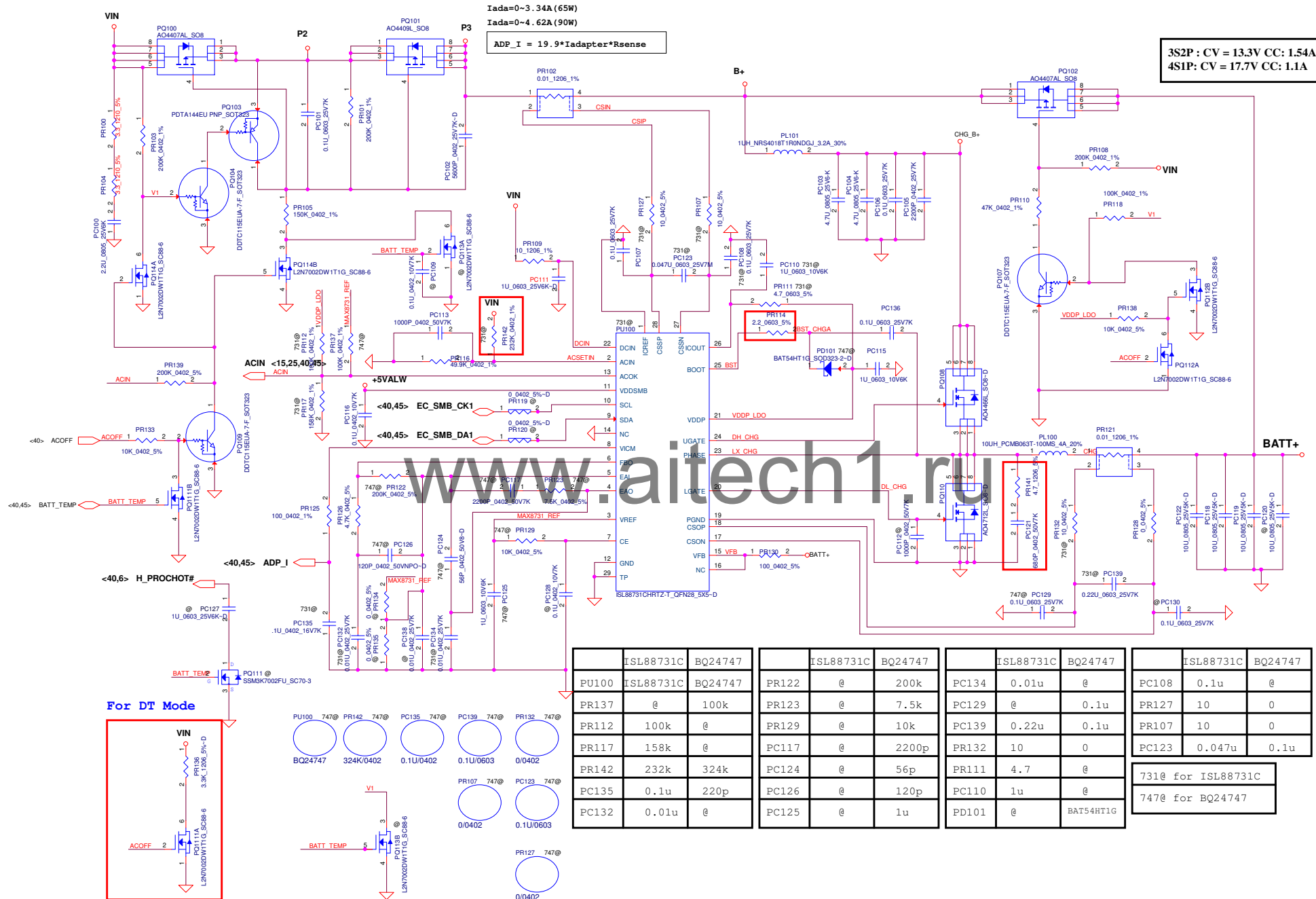
Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	34	Card Reader	2012/04/27	HW	The Card reader USB signal is incorrect.	SWAP UR1 USB signal P/N	0.2
2	40	Keyboard	2012/05/03	SED	Keyboard pin define change.	Follow new SPEC.SWAP JKB pin define.	0.2
3	16,21,34,36,37,38	USB	2012/05/04	Function team	Change USB port assignment for function team request	USB port change detail please reference Page.16 description.	0.2
4	26	VGA	2012/05/05	HW	Delete reserve BACO circuit	Delete UV15,QV16,QV17,QV18,QV19,QV20,RV99,RV100,RV249,CV96,CV98	0.2
5	42	DC/DC	2012/05/07	HW	Design change	UN-POP R211, POP R217	0.2
6	33	Audio codec	2012/05/09	ESD	ESD team ask solution	Add RA29,RA30,RA31,RA32 and place on the moat between GND & GNDA	0.2
7	6,17	PCH	2012/05/09	ESD	ESD team ask reserve solution	Add CC151,CH102 for reserve	0.2
8	32	LAN	2012/05/10	HW	Remove China Go-rural for DELL request	Remove DL7,DL8,DL9	0.2
9	16,38	USB	2012/05/10	HW	Remove JUSB3 USB3.0	Delete LI8,LI9,DI6 and change JUSB3 to USB2.0 type	0.2
10	32	Crystal	2012/05/15	HW	Crystal vendor suggestion	Change CL36,CL37 from 33p/0402 to 12p/0402	0.2
11	21,39	LVDS	2012/05/17	SED	Add FHD Panel CE_ENABLE, DBC_ENABLE function from SED request	Add CE_EN, DBC_EN control pin to EC	0.2
12	21	LVDS	2012/05/22	SED	Follow SED team request disable CE_EN function	Change RV62 to DE-POP and RV100 to POP for disable CE_EN function	0.2
13	33	Audio codec	2012/05/23	CODEC	Follow CODEC vendor suggestion	Add AUDIO JACK PLUG delay circuit, Spearate NET JACK_PLUG to -> JACK_SENSE# & "> JACK_PLUG#	0.2
14	16,21	Touch Screen	2012/05/29	HW	Add touch screen function	Add RV217, RV218, RV219, RV249, CV59, CV60, CV328, DV13, QV16, JTOUCH	0.2
15	39	Board ID	2012/05/30	HW	Board ID change for PT	Change RE5 from 8.2k_0402(SD028820180) to 33k_0402(SD028330280)	0.2
16	21,39	Touch Screen	2012/05/30	HW	Add touch screen function power control	Add NET "TOUCH_ON#" from JTOUCH to UE1.82(KB9012) for TOUCH SCREEN PANEL power control	0.2
17	33	Audio codec	2012/05/30	HW	Follow RealTek suggestion remove, delete reserve MUTE circuit	Delete D1,QAI,QA2,QA3,RA24,RA26,RA60,RA62,RA68,RA109,CA72,CA73	0.2
18	15,16,39,41	ESD	2012/05/30	ESD	ESD ask CAP for reserve	Reserve 0.1u/0402 CH104,CZ23,CH105,CE27,CE28	0.2
19	14	Green CLK	2012/05/30	HW	For Green CLK test	Change RH31,RH41,RV232 0ohm form "GCLK#" to "g" for break the clock signal to device	0.2
20	10,26,41	DC/DC	2012/05/31	HW	Change "+1.5V_CPU_VDDQ", "+1.5VS", "+1.5VGS" derating	Change RC150 33k/0402 to 2M/0402, RC151 100K/0402 to 470K/0402, R238 100K/0402 to 470K/0402, RV115 0/0402 to 2M/0402	0.2
21	41	DC/DC	2012/05/31	HW	For power sequence tuning	Change R215 to DE-POP	0.2
22	06,15,16,39,41	ESD	2012/05/31	ESD	Follow ESD team request	Change 0.1u/0402 from "g" to POP	0.2
23	32	Green CLK	2012/06/15	HW	Change for Green CLK bom control	Change RL21,RL30 from "g" to "GCLK#"	0.2
24	41	DC/DC	2012/06/15	HW	For WLAN card power sequence issue	Change R24,R213 from 470K/0402 56K/0402	0.2
25	35,41	Schematic page modify	2012/06/18	HW	Schematic page modify for easily maintain.	Swap Page. 35 & Page 41.	0.2
26	41	ODD	2012/06/18	HW	Change component location for easily maintain.	Move RH42,RH43 from Page.13 to Page.41.	0.2
27	39	FAN	2012/06/29	HW	Fan speed noise issue	Reserve 220p/0402 CE24	0.3
28	6	CPU	2012/06/29	ESD	System boot-up shot down issue.	Change CC151 from POP to "g"	0.3
29	21,35,39,40,41	Circuit adjust	2012/07/01	HW	Circuit & page adjust for OAK 15" & OAK 17"	1. Swap P.35 & P.41and move touch screen circuit from P.21 to P.41. 2. Swap P.39 & P.40 page no	0.3
30	40	LID SW	2012/07/01	HW	LID SW need a trace for debug and switch.	Add RE81 for LID SW.	0.3
31	25	GPU	2012/07/01	HW	Follow AMD request, MarsPro will used MPLs.	Change RV75,RV76,RV81 from "DIS#" to "TH#"	0.3
32	29	GPU	2012/07/01	HW	Follow AMD request, MEM_CALRP2 is not need for Mars ASIC now.	Change RV205 from "MS#" to "g"	0.3
33	38	MINI card	2012/07/03	HW	Power Control for Mini card didn't need	Change R17 to "g"	0.3
34	6	XDP	2012/07/06	HW	S3 return hang issue	Change RC89 from "g" to POP	0.3
35	23	GREEN CLK	2012/07/09	HW	Follow Green CLK FAE suggestion	1. Change UG1.2(+3VLP) & UG1.8(+3VALW) connect to +LAN_IO 2. Add R787 connect from +RTCBATT to C5.2 & UG1.10 3. Change C14 from 0.1u to 5p/0402 4. Change C8 connect from +3V_ALW to +LAN_IO 5. Add R788 0ohm/0402 from +RTCVCC to UG1 for GCLK & DH1 select	0.3
36	35	MOAT	2012/07/09	ESD	For ESD request reserve CAP.	Reserve those CAP for ESD MOAT.	0.3
37	18	LVDS	2012/07/10	HW	Change RES and reserve CAP for LVDS issue	Change RH185 from 0ohm-short to 0ohm/0805, and reserve CH106 1U/0402	0.3
38	41	Connector	2012/07/10	ME	For ME request	Change JBTB1 footprint from SP02000G800 (OLD) to SP02000MJ00	0.3
39	13	PCH	2012/07/11	ESD	Follow ESD team request	Add RH44,RH48,RH70 & NET PCH_JTAG_TMS_R, PCH_JTAG_TDI_R, PCH_JTAG_IDO_R for break signal trace	0.3
40	40	PCH	2012/07/11	ESD	Follow ESD team request	1. Change NET NAME "N59110727" to "WL_BT_LED#_R" 2. Reserve 0.1u/0402 on "WL_BT_LED#_R" for ESD	0.3
41	21	LVDS	2012/07/11	HW	Reserve for CE function for LVDS connector	Change CE_EN_R from dummy to JLVD5.18	0.3

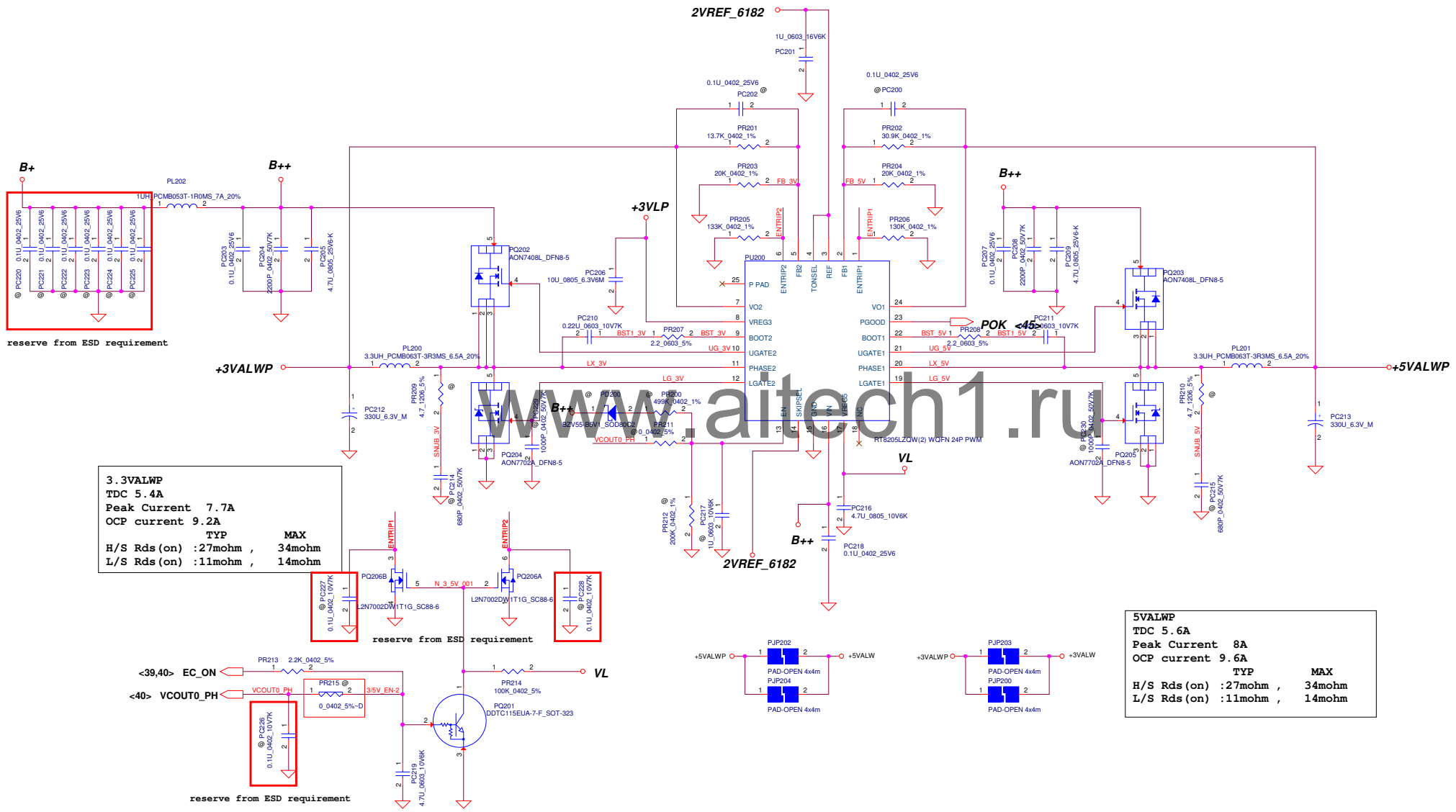
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HW-PIR				Rev. 0.4
LA-9101P				Date: Wednesday, August 28, 2012 Sheet 43 of 57

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
40	32	Connector	2012/07/12	ME	For ME request	Change JLAN CPN from "DC234004V00" to "SP011207090"	0.3
41	40	FAN	2012/07/16	HW	For FAN_SPEED1 noise issue	Change CE29 from "@" to POP	0.3
42	14	Touch PAD	2012/07/17	SED	Change Touch PAD SMBUS port for SMBUS issue	Change Touch PAD SMBUS port for SMB0 to SMB	0.4
43	32	GREEN CLK	2012/07/19	HW	Follow Silago FAE request	Change RL21 from 510 ohm to 0 ohm/0402	0.4
44	41	Touch Screen	2012/08/07	SED	Follow SED team request change JTOUCH USB signal conatct.	Change JTOUCH Pin define.	0.4
45	34	Card Reader	2012/08/14	ESD	Follow ESD team request	Reserve CR11 100p/0402 close to JREAD	0.4
46	23	GREEN CLK	2012/08/16	HW	Fixed GCLK output abnormal issue	Change UG1.2(UG1/VDD) from +LAN_IO to+3VALW	0.4
47	33	CODEC	2012/08/16	HW	The issue already fixed by new CODEC.	Remove delay circuit and POP RA4	0.4
48	23	GREEN CLK	2012/08/17	HW	For RTC discharge issue	De-pop R788	0.4
49	32,34	LAN	2012/08/17	HW	For LAN Chip abnormal leakage issue	Pop RL34 and de-pop RE21	0.4
50	34	Card Reader	2012/08/20	ESD	Follow ESD team request	Change CR11 from 100p/0402 to 10p/0402 and POP	0.4
51	41	Touch Screen	2012/08/20	SED	Follow SED team request	Change Touch screen power rail for +3VS to +5VS	0.4
52	38	LED	2012/08/20	HW	Change LED light	Change LED1,LED2,LED4 CPN from SC500006000 to SC50000DC00	0.4
53	38	WLAN	2012/08/20	HW	Remove AQAC function power control	Change R18,R19,R20,R21,C13,Q2,Q4 component BOM structure to "@"	0.4
54	41	Touch Screen	2012/08/20	HW	Add EC control for Touch Screen function	Add RN15 & QN6 and relative circuit connect	0.4

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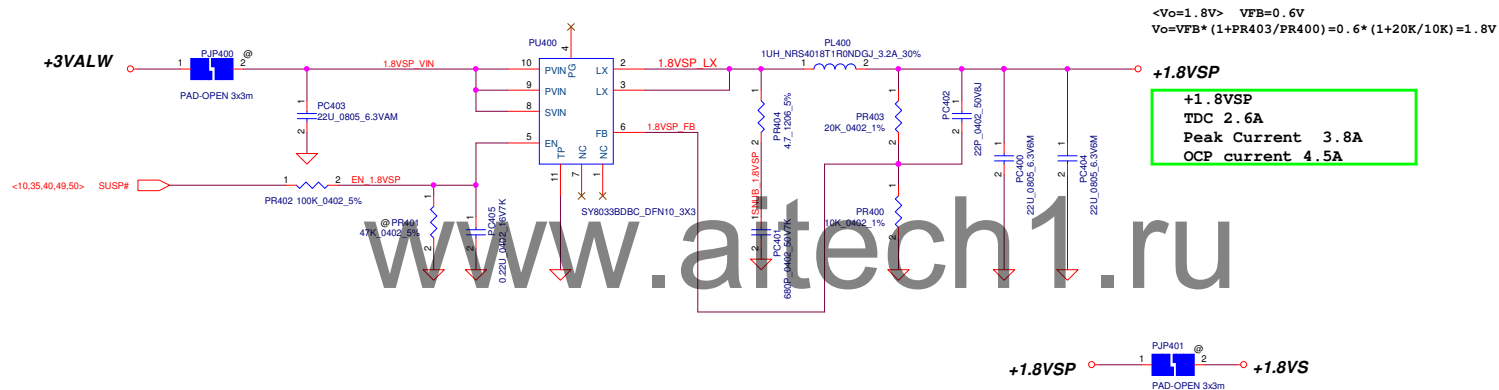
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Document Number				Rev	
LA-9101P				0.4	
Sheet				44 of 57	

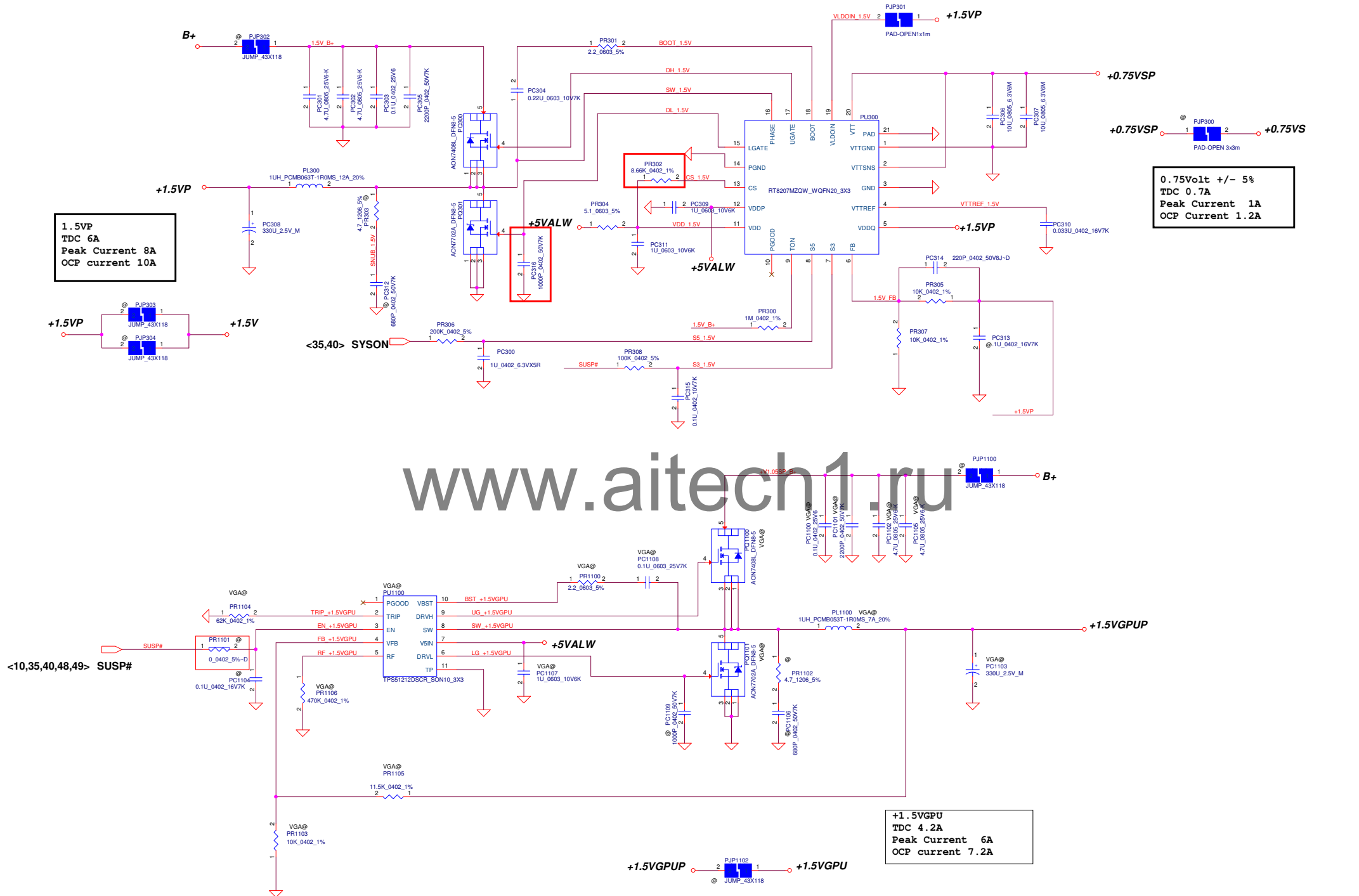




3.3VALWP
TDC 5.4A
Peak Current 7.7A
OCP current 9.2A
TYP
H/S Rds (on) : 27mohm , 34mohm
L/S Rds (on) : 11mohm , 14mohm

5VALWP
TDC 5.6A
Peak Current 8A
OCP current 9.6A
TYP
H/S Rds (on) : 27mohm , 34mohm
L/S Rds (on) : 11mohm , 14mohm

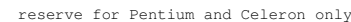
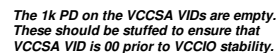


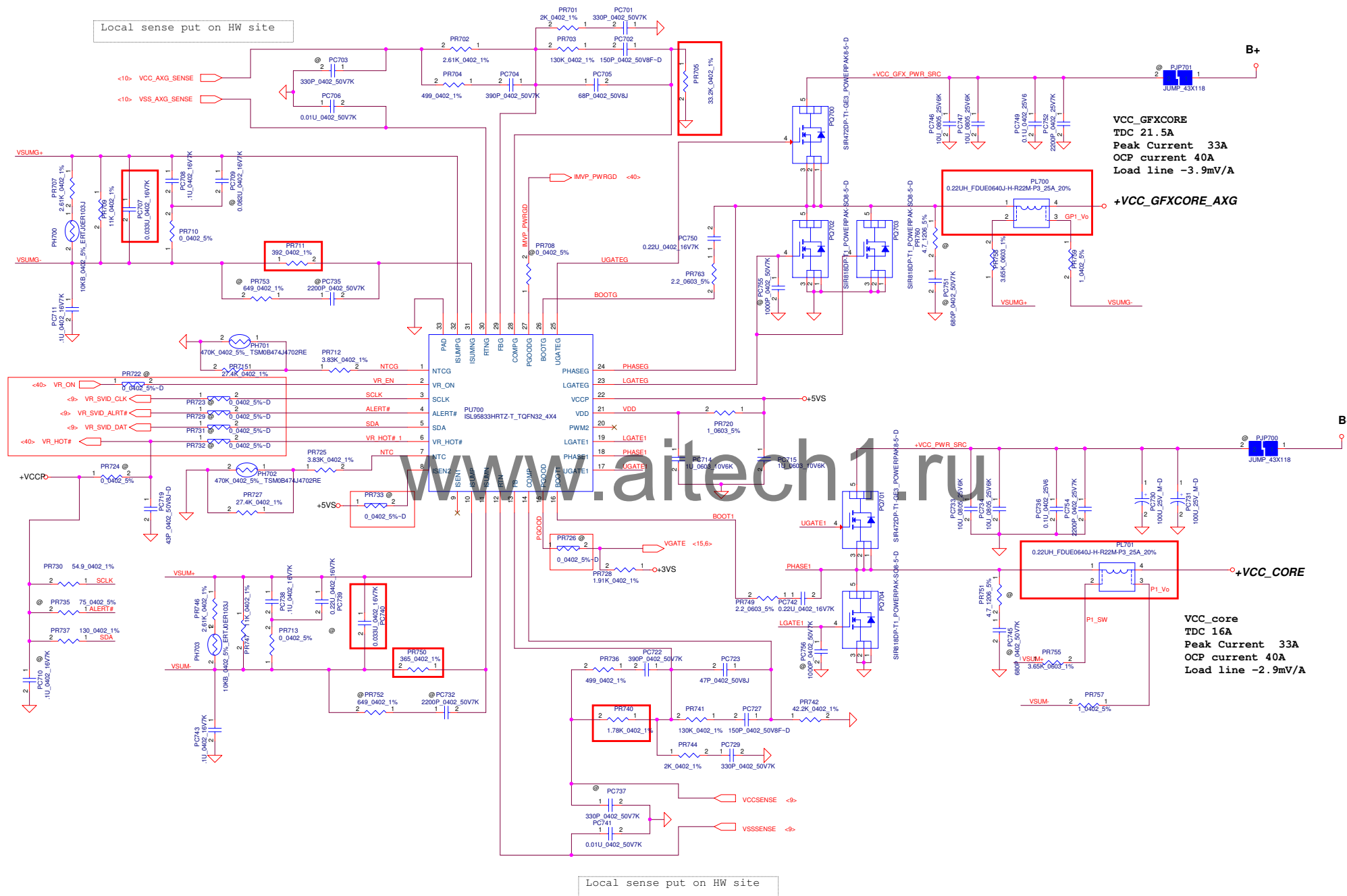


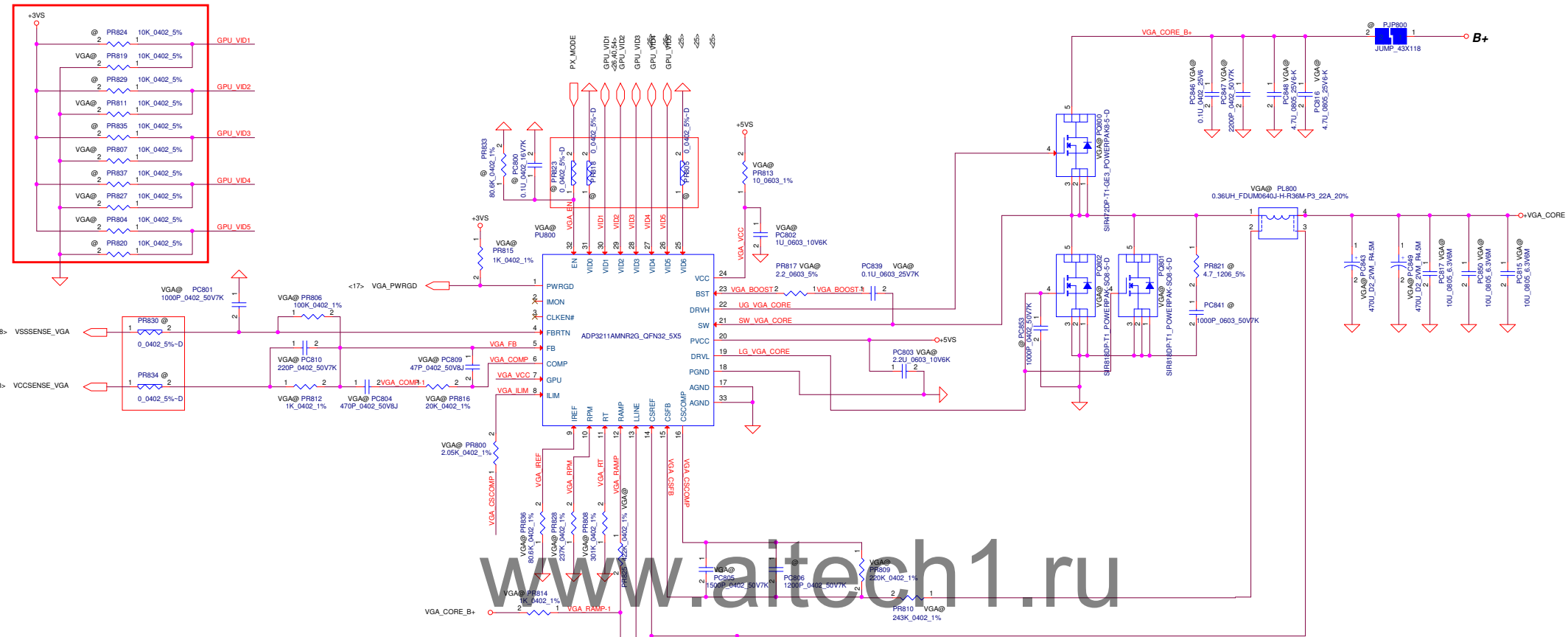
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				Date	Wednesday, August 28, 2012
				Sheet	50 of 57

output voltage adjustable network







Mars Pro

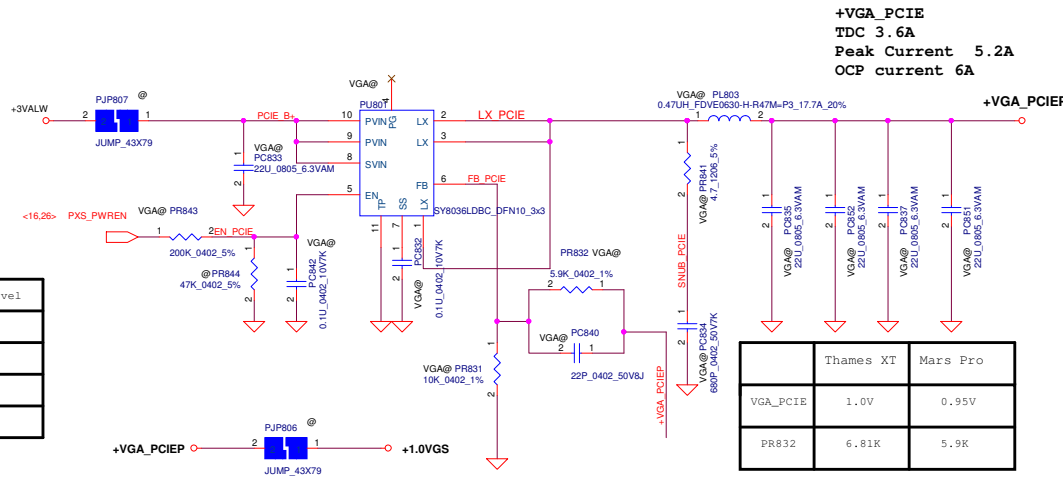
GPU_VID5 (GPIO_10)	GPU_VID4 (GPIO_14)	GPU_VID3 (GPIO_15)	GPU_VID2 (GPIO_16)	GPU_VID1 (GPIO_20)	Core Voltage Level
0	1	1	1	1	1.125V
1	0	0	0	0	1.1V
1	0	0	0	0	1.075V
1	0	0	1	0	1.05V
1	0	0	1	1	1.025V
1	0	1	0	0	1V
1	0	1	0	1	0.975V
1	0	1	1	0	0.95V
1	0	1	1	1	0.925V
1	1	0	0	0	0.9V
1	1	0	0	1	0.875V
1	1	0	1	0	0.85V
1	1	0	1	1	0.825V
1	1	1	0	0	0.8V

+VGA_CORE
TDC 22A
Peak Current 30A
OCP current 36A
FSW=350kHz
DCR 1.1mohm +/-5%
Loadline = 1.5mohm

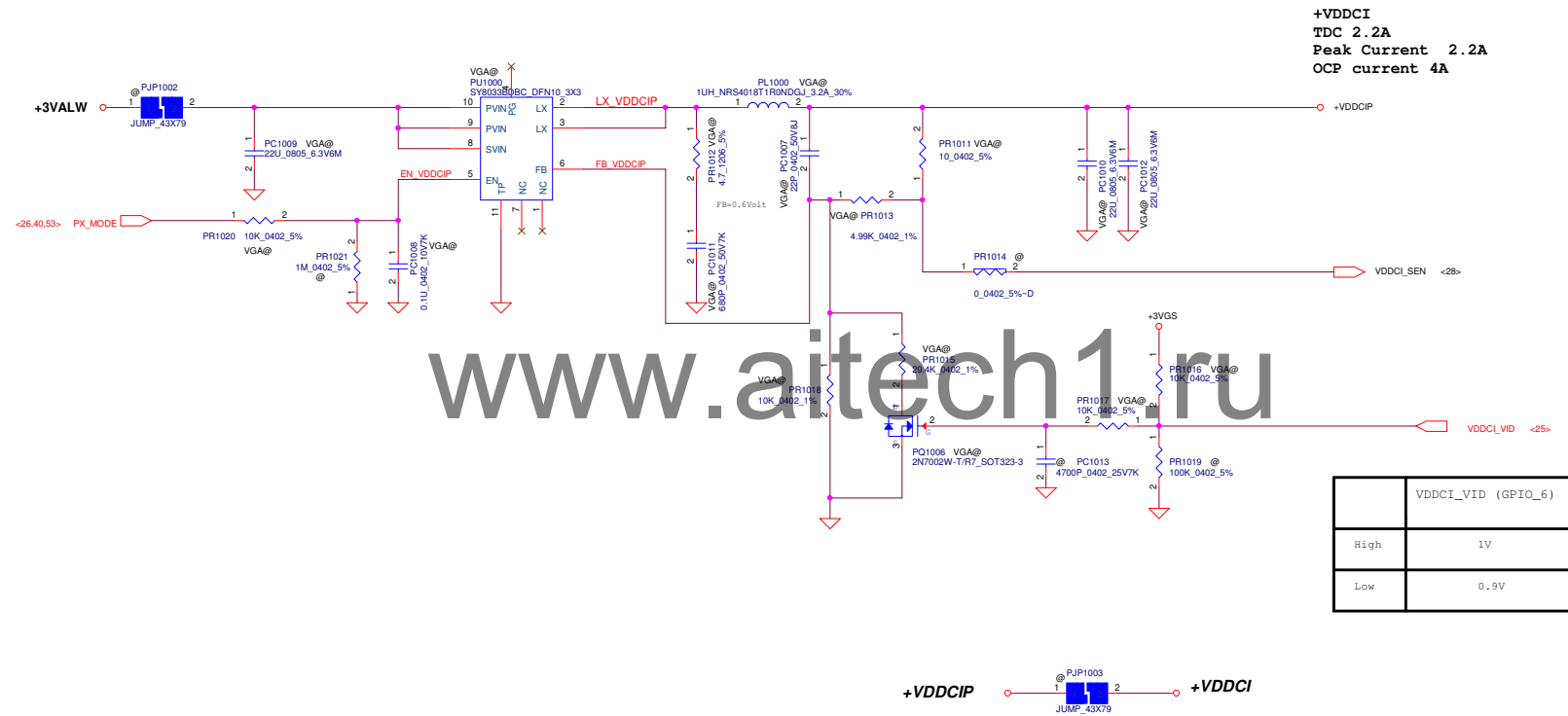
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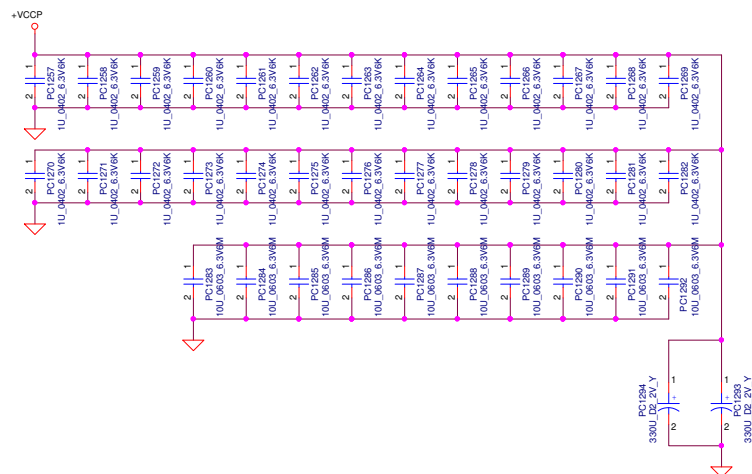
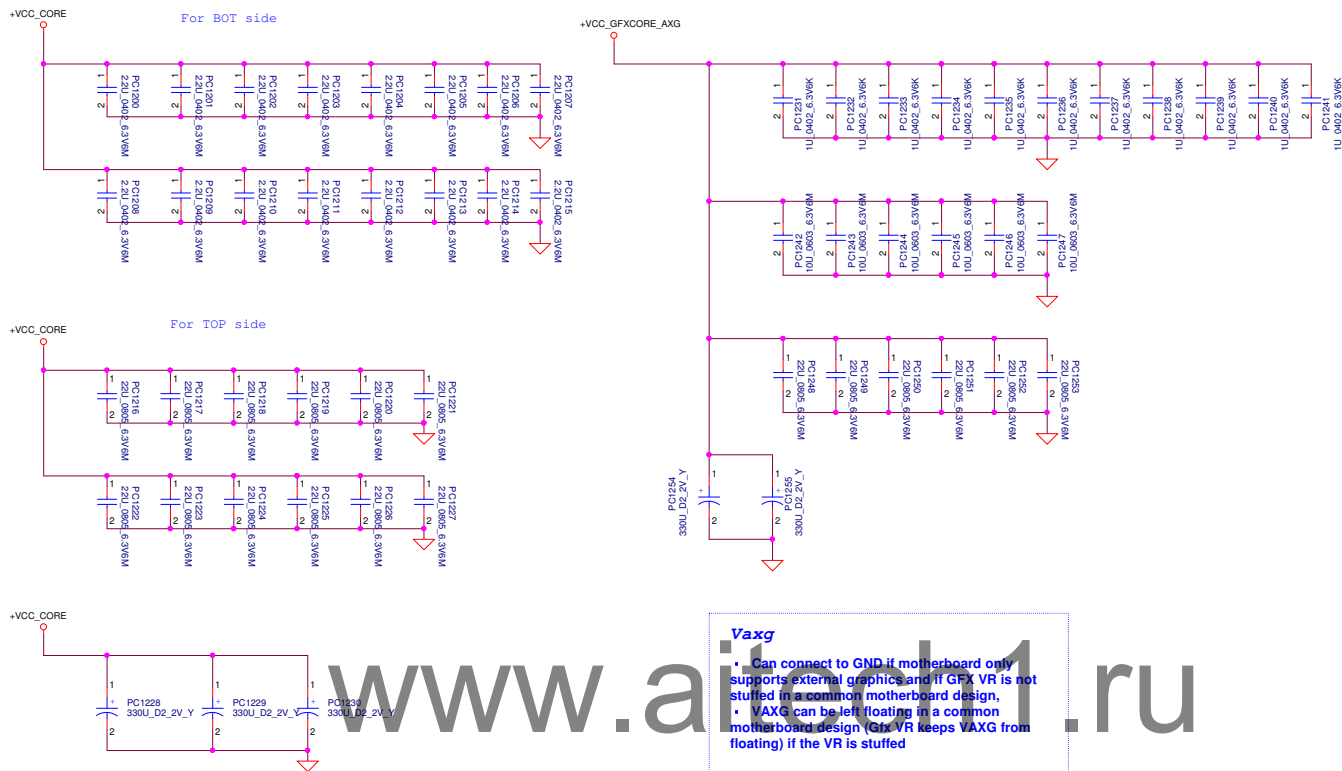
GPU_VID5 (GPIO_10)	GPU_VID4 (GPIO_14)	GPU_VID3 (GPIO_15)	GPU_VID2 (GPIO_16)	GPU_VID1 (GPIO_20)	Core Voltage Level
1	0	0	1	0	1.05V
1	0	1	0	0	1V
1	0	1	1	0	0.95V
1	1	0	0	0	0.9V

+VGA_CORE
TDC 20A
Peak Current 30A
OCP current 36A
FSW=350kHz
DCR 1.1mohm +/-5%

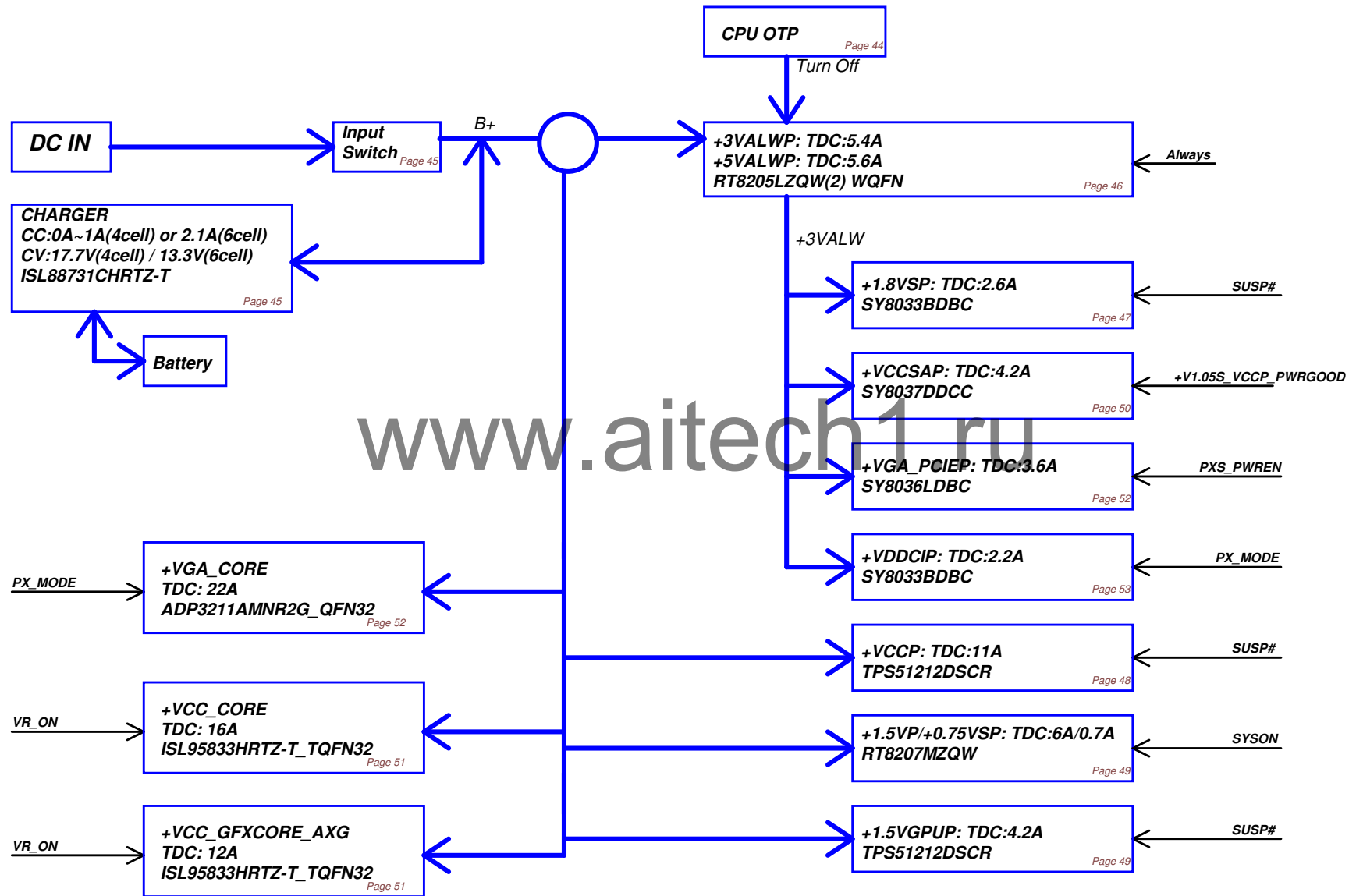


	Thames XT	Mars Pro
VGA_PCIE	1.0V	0.95V
PR832	6.81K	5.9K





Power block



Version Change List (P. I. R. List)

Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	51	VCORE	12/05/11	Morris	adjust VR parameter	change PL700 and PL701 from 0.36u to 0.22u change PC707 and PC740 from 0.047u to 0.033u change PR750 from 649 to 365 change PR711 from 649 to 392 change PR740 from 1.91k to 1.78k change PR705 from 150k to 33.2k	X00
2	44 45 46	DCIN/BATT CONN/OTP CHARGER 3.3VALWP/5VALWP	12/05/11	Morris	follow SSI memo for part shortage issue	change PQ112,PQ114,PQ1111,PQ206,PQ904 from SB00000CQ00 to SB00000PV00	X00
3	49	+1.5VP/1.5VDGPU/0.75VSP	12/05/15	Morris	design change	change PR302 from 12k to 8.66k	X00
4	50	+VCCSAP	12/05/23	Morris	for Pentium and Celeron special BOM	add PR607 and reserve	X00
5	49	+1.5VP/1.5VDGPU/0.75VSP	12/07/06	Morris	design change to reduce low-side mosfet induce	add PC316 1000pf	X01
6	45	CHARGER	12/07/17	Morris	from EMI request	change PR114 from 0 to 2.2 add PR141 and PC121	X01
7	45	CHARGER	12/07/17	Morris	design change to solve Battery LED is still on after unplug AC when SUT in S3S4S5 issue	change PR142 from 210k to 232k for ISL88731C (X76) change PR142 from 309k to 324k for BQ24747 (X76)	X01
8	44	DCIN/BATT CONN/OTP	12/07/17	Morris	revise OTP setting to 96C from thermal request	change PR927 from 12.1k to 11k	X01

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Issued Date	2012/08/22	Deciphered Date	2013/07/31	Title	PWR-PIR
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				Date	Wednesday, August 28, 2012
				Sheet	57 of 57
				Rev	0.4